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Analysis of a Complementary Amplifier Useful for High Slew Rate Applications

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I am submitting herewith a thesis written by Dick Ray Fletcher entitled "Analysis of a Complementary Amplifier Useful for High Slew Rate Applications." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

E.J. Kennedy, Major Professor

We have read this thesis and recommend its acceptance:

Lewis Nelson, W.J. McClain

Accepted for the Council:

Dixie L. Thompson

Vice Provost and Dean of the Graduate School

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100
November 29, 1971

To the Graduate Council:

I am submitting herewith a thesis written by Dick Ray Fletcher entitled "Analysis of a Complementary Amplifier Useful for High Slew Rate Applications." I recommend that it be accepted for nine quarter hours of credit in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

E. A. Kennedy
Major Professor

We have read this thesis and
recommend its acceptance:

Lewis Nelson

W. J. McClain

Accepted for the Council:

Hilton A. Smith
Vice Chancellor for
Graduate Studies and Research

ANALYSIS OF A COMPLEMENTARY AMPLIFIER USEFUL
FOR HIGH SLEW RATE APPLICATIONS

A Thesis
Presented to
the Graduate Council of
The University of Tennessee

In Partial Fulfillment
of the Requirements for the Degree
Master of Science

by
Dick Ray Fletcher
March 1972

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ABSTRACT

Operational amplifiers which are utilized in applications involving the amplification of high-frequency signals and fast rise-time pulses must have a high slew rate and a wide bandwidth. Integrated circuit, particularly thin-film hybrid, amplifiers with wide bandwidths can be readily obtained; however, monolithic IC's are not readily available with as large a slew rate as can be obtained with discrete-device amplifiers.

The goal of this thesis was to investigate the design of an amplifier using a complementary output stage with the objectives of obtaining low quiescent power dissipation, a slew rate equivalent to the small-signal bandwidth of the amplifier, and a closed-loop gain of 10. The circuit was constructed and tested experimentally, and the results indicated that a slew rate of 200 volts per μ sec could be obtained using a single complementary output stage.

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CHAPTER I

INTRODUCTION

Operational amplifiers are currently being utilized to a large degree in applications which require the amplification of high-frequency signals and fast rise-time pulses, and also as line drivers to transmit wideband data over transmission lines. The performance characteristics of operational amplifiers which can be used for these applications are very much different from the amplifiers previously used as relatively slow-speed analog computing elements (1)*.

The performance characteristics of operational amplifiers used as analog computing elements are very well defined in Reference 2. Aside from these basic criteria of operational amplifiers, the slew rate and bandwidth become very important parameters if the amplifier is to be used in wideband data and line driver applications (3). For this thesis the definition of slew rate is the ratio of the total large-signal output voltage change to the time required for the change. The bandwidth is defined as that frequency at which the closed-loop gain of the amplifier has decreased 3 decibels (db) from the midband frequency gain.

Although monolithic IC operational amplifiers are competitive with discrete component operational amplifiers in relation to some performance characteristics, the discrete component amplifiers are superior

*Numbers in parentheses refer to similarly numbered items in the List of References.

to the IC amplifiers in wide bandwidth and fast slew rate applications (3, 4, 5). Monolithic IC amplifiers are becoming available with bandwidths which rival that of discrete component amplifiers (2); however, the slew rate of discrete component and hybrid IC amplifiers remain far superior, 10 to 100 times faster, than that of the monolithic IC amplifiers.

The driver or output stage of the amplifier, which must be able to supply a bipolar output voltage, usually limits the minimum large-signal rise time of the amplifier. It is in the output stage that the largest voltage and current transitions occur, therefore the ability of the output stage to switch between these voltage and current extremes usually determines the slew rate of the amplifier (6, 7).

The use of a complementary pnp and npn transistor pair in the output stage of the amplifier offers the advantages of circuit simplicity, no phase inversion for bipolar outputs, and equal loads for the driver transistor on both positive and negative outputs. Discrete pnp and npn complementary transistors capable of providing high current drive and wide frequency response are readily available. However, the difficulties involved in fabricating a high-gain pnp monolithic IC transistor to operate as a complementary pair with a npn transistor, that is to provide symmetrical current gain, are considerable and expensive. The lateral pnp transistor can be economically fabricated in a monolithic IC; however, the frequency performance and current gain deviate too far from that of the npn to form a good complementary pair (4). A vertical pnp transistor could be fabricated but it requires

additional fabrication steps and process controls to obtain an acceptable current gain and breakdown voltage (4, 8).

The difficulty and expense involved in the production of monolithic IC pnp transistors with good performance characteristics has led to the use of quasicomplementary output stages in many monolithic IC amplifiers. The quasicomplementary configuration utilizes the economical lateral pnp and a npn connected in a configuration which provides the characteristics of a high current gain pnp transistor (4, 8, 9).

Scope of the Thesis

The purpose of this thesis is to investigate a complementary amplifier with a wide bandwidth and a high slew rate which could be used in a hybrid, thin or thick-film, configuration with an IC amplifier. The thesis will be limited to an output stage similar to that of the Fairchild μ A709 monolithic IC amplifier.

The design goals of the thesis are to provide an amplifier with (1) an output whose small-signal and large-signal rise time are approximately 10 nsec, (2) good linearity, (3) low quiescent power dissipation and (4) a ± 5 volt drive into a 100-ohm load.

It is difficult to find published work which deals with the slew rate and bandwidth problem in the basic complementary amplifier. The operational amplifiers which have high slew rates and wide bandwidths are discrete device amplifiers and the techniques used by the manufacturers are usually considered confidential by the manufacturers.

Chapter II presents an analysis of the slew rate and bandwidth characteristics of the basic complementary amplifier chosen for this investigation. A method of improving the slew rate is described in Chapter III.

The experimental results are presented in Chapter IV.

Chapter V contains a brief summary of the material presented in this thesis, along with the conclusions reached.

CHAPTER II

THE BASIC COMPLEMENTARY-SYMMETRY AMPLIFIER

When an amplifier is used in an application requiring the amplification of wideband data, pulses, and line driving ability, the open-loop bandwidth and slew rate become important operating characteristics of the amplifier. The output stage of the amplifier must provide the necessary voltage swings and current drive without decreasing the bandwidth and without producing a slew rate limiting effect on the output signal.

IC operational amplifiers of the Fairchild $\mu A709$ type have utilized the pnp and npn complementary-symmetry output stage. The output stage of the $\mu A709$, shown in dotted lines in Figure 1, consists of the transistors Q_9 and Q_{12} through Q_{14} and resistors R_7 , R_{12} , R_{13} , R_{14} , and R_{15} . The increase and decrease of collector current in transistor Q_{12} and associated voltage drop on resistor R_{14} provide the necessary voltage swings at the collector of Q_{12} for the proper conduction of transistors Q_{13} and Q_{14} , the output drivers.

A schematic of the basic complementary amplifier utilized for this thesis is shown in Figure 2. The differential input stage of the amplifier was chosen instead of the common base input, Q_9 of Figure 1, to provide a convenient means of feedback, a means for adjusting the output voltage to zero volts with the input equal to zero volts and for stability of this bias condition, and to prevent loading of the input

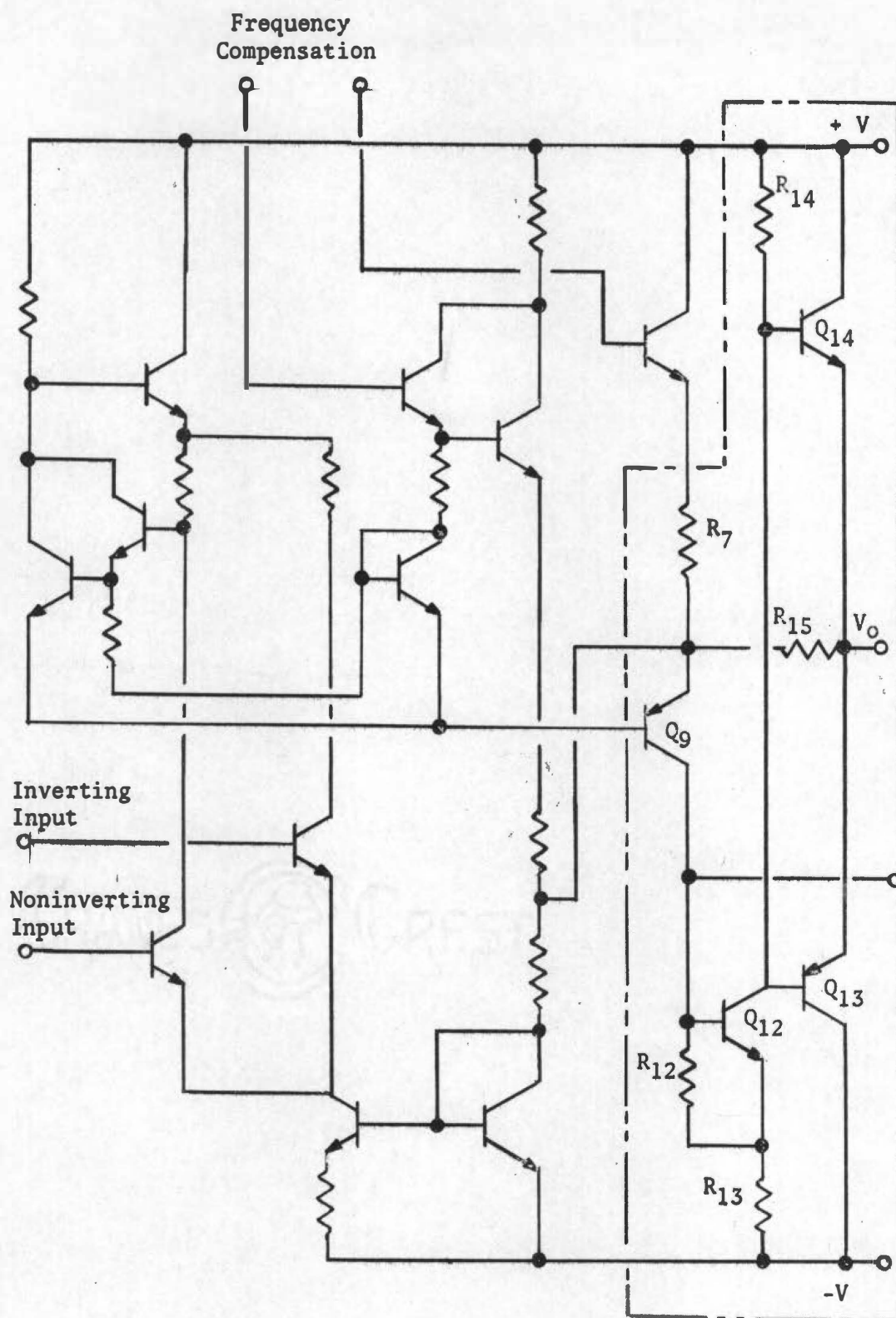


Figure 1. Fairchild $\mu A709$ amplifier.

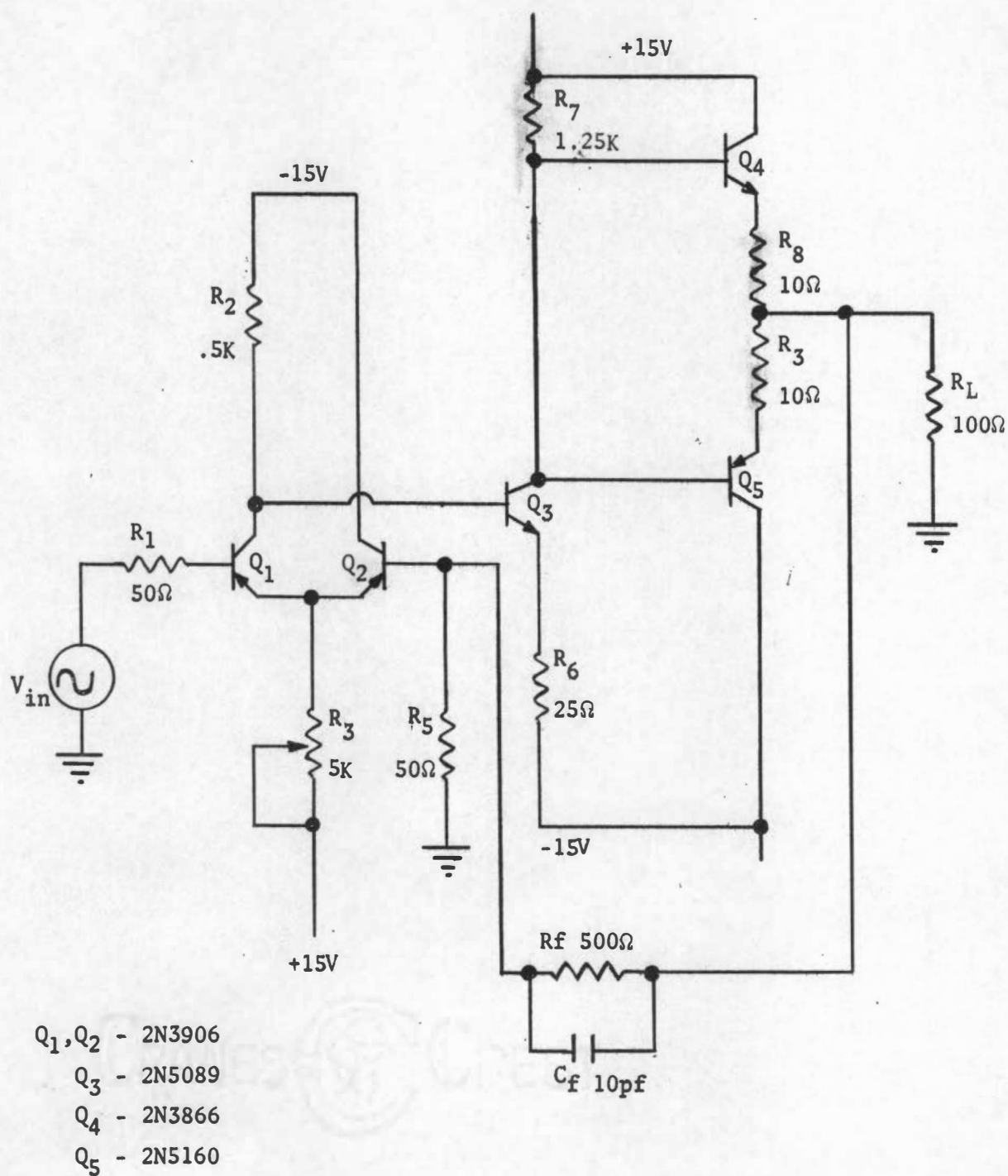


Figure 2. Basic complementary amplifier.

signal (10, 11). Transistors Q_1 and Q_2 are inexpensive epoxy high-frequency devices.

Transistor Q_3 is a high current-gain amplifier with a relatively high current gain-bandwidth product (f_T). Other characteristics of Q_3 which contributed to its choice as the predriver stage are high collector-to-base breakdown voltage (BV_{CBO}), relatively low base-to-collector capacitance (C_{μ}), and a practically constant current gain (h_{FE}) over a wide range of operating currents.

Transistors Q_4 and Q_5 , Figure 2, are high-frequency devices with adequate current and power capacity. The 2N3866 and 2N5160, Q_4 and Q_5 , have been used successfully (6, 12) as a good complementary pair. Q_4 and Q_5 are matched as closely as possible with regard to h_{FE} to reduce distortion of the output voltage (13).

Slew Rate Calculations

The slew rate of the amplifier shown in Figure 2 is limited by the rate at which the capacitance at the collector of Q_3 can be charged (6). The relationship for voltage and capacitance (14) is given by

$$V = \frac{Q}{C_T} , \quad (1)$$

where V is the voltage at the collector of transistor Q_3 , C_T is the total capacitance at the collector of Q_3 , and Q is the associated charge.

The total capacitance at the collector of transistor Q_3 is given approximately by (10)

$$C_T = C_{\mu 3} + C_{\mu 4} + C_{\mu 5} + C_S , \quad (2)$$

where $C_{\mu 3}$, $C_{\mu 4}$, and $C_{\mu 5}$ are the collector-to-base capacitance (15) of the respective transistors, and C_S is the stray capacitance at the collector of transistor Q_3 . The values of C_{μ} as obtained from the transistor specification sheets are

$$C_{\mu 3} = 1.7 \text{ pf} .$$

$$C_{\mu 4} = 3 \text{ pf} .$$

$$C_{\mu 5} = 3 \text{ pf} .$$

A value of 3pf was assumed for the stray capacitance. The value of C_T then from Equation 2 is

$$C_T = 1.7 \text{ pf} + 3 \text{ pf} + 3 \text{ pf} + 3 \text{ pf} .$$

$$C_T = 10.7 \text{ pf} .$$

Assuming that the capacitance at the collector of transistor Q_3 is not a function of the voltage at that point, we have from Equation 1

$$\frac{\Delta V}{\Delta t} = \frac{1}{C_T} \frac{\Delta Q}{\Delta t} , \quad (3)$$

where $\frac{\Delta Q}{\Delta t}$ is the current required in the capacitance C_T to produce the slew rate, $\frac{\Delta V}{\Delta t}$.

The initial design constraints for this amplifier were to obtain a small-signal rise time of 10 nsec, equivalent to a -3db bandwidth of approximately 35 MHz (11), and a slew rate sufficient to obtain the same rise time of 10 nsec for an output drive of ± 5 volts into a load resistor of 100 ohms. Thus, the slew rate at the output of the amplifier would be 5 V/10 nsec, or 500 V/ μ sec. A slew rate of approximately 6 V/10 nsec will be required at the collector of Q_3 in Figure 2, page 7, because of the voltage drop on R_8 or R_3 . Making the substitution into Equation 3

$$\frac{6V}{10 \text{ nsec}} = \left(\frac{1}{10.7 \text{ pf}} \right) \frac{\Delta Q}{\Delta t} = \frac{1}{10.7 \text{ pf}} i$$

Solving for i

$$i = 10.7 \times 10^{-2} \left[\frac{6}{10^{-8}} \right]$$

$$i = 6.42 \text{ ma.}$$

This is the current required to charge the capacitance at the collector of transistor Q_3 for an output slew rate of 500V/ μ sec. This does not include the current through the resistor R_7 which must be supplied to develop the 6V change at the collector of Q_3 .

A quiescent current of 12 ma was chosen for transistor Q_3 , Figure 2, page 7, to insure that Q_3 would remain well above cut-off when the collector current of Q_3 decreased by the amount required for the proper slew rate, plus that required for the decreased voltage drop on R_7 for the proper output voltage level. The value of R_7 can then be

calculated, with the output at zero volts, as

$$R_7 = \frac{15V}{12ma} = 1.25K .$$

The maximum required collector current through Q_3 would occur on the -5V output voltage and can be taken as a worse case to be

$$I(Q_3)_{Max} = \frac{(+V_{cc} + 6V)}{R_7} + i + i_{BQ_5} \quad (4)$$

where i_{BQ_5} is the base current drive required by transistor Q_5 in Figure 2, page 7, for the 50 ma output current. The value for i_{BQ_5} is given by (10, 14, 15)

$$i_{BQ_5} = \frac{i_{CQ_5}}{h_{FE}} \approx \frac{i_{EQ_5}}{h_{FE}} \quad (5)$$

where i_{CQ_5} and i_{EQ_5} are the respective collector and emitter currents of transistor Q_5 . Using the value for i calculated from Equation 3 and the measured value for h_{FE} of transistor Q_5 , substitution into Equation 4 gives

$$I(Q_3)_{Max} \approx \frac{21V}{1.2K} + 6.42 \text{ ma} + \frac{50 \text{ ma}}{40} .$$

$$I(Q_3)_{Max} \approx 17.5 \text{ ma} + 6.42 \text{ ma} + 1.25 \text{ ma} .$$

$$I(Q_3)_{Max} \approx 25.17 \text{ ma} .$$

The 2N5089 is rated with a maximum collector current of 50 ma. Also, the maximum instantaneous power which would be dissipated by Q_3 is given by (16)

$$P_D = V_{CE} I_C ,$$

or

$$P_D = 9V (25.17 \text{ ma}) = 226 \text{ mw.}$$

The rated average total device dissipation for the 2N5089 is given as 310 mw at an ambient temperature of 25°C. Hence, the calculated value of P_D is safely within the rated average value.

The minimum current through Q_3 , Figure 2, page 7, occurs for a positive output drive of 5 volts, or approximately 6 volts at the Q_3 collector. Here, transistor Q_4 conducts, and $I(Q_3)_{\text{Min}}$ is

$$I(Q_3)_{\text{Min}} \approx \frac{15V}{R_7} - [i_{BQ_4} + i + \frac{6V}{R_7}] ,$$

or, substituting values with $h_{FE}(Q_4) \approx h_{FE}(Q_5)$,

$$I(Q_3)_{\text{Min}} \approx 0.06 \text{ ma.}$$

Thus, Q_3 would essentially be cut-off if a slew rate of 500 V/μsec at the output were achieved. In actuality, as the current through Q_3 is reduced, the attainable slew rate, for positive drive at the output, is reduced. Thus, it would be very improbable to obtain 500 V/μsec slew rate for positive output drive for the circuit of Figure 2, page 7.

Because of the voltage gain from the base-to-collector of transistor Q_3 in Figure 2, page 7, the slew rate requirement at the base of Q_3 will be considerably less than that at the collector. The slew rate required at the base of transistor Q_3 is

$$SR_3 = \frac{6V/Avt_3}{10 \text{ nsec}} , \quad (6)$$

where Avt_3 is the voltage gain of Q_3 . In the accompanying section on Gain and Bandwidth, page 14, the computed voltage gain of Q_3 is 34.3. The required slew rate at the input to Q_3 is, by substitution into Equation 6, equal to 17.5 V/ μ sec.

The required current for a slew rate of 17.5 V/ μ sec at the input to Q_3 , Figure 2, page 7, can be calculated using Equation 3. Therefore

$$I_{\text{req'd}} \geq C_{B3} (17.5 \text{ V}/\mu\text{sec}) + i_{BQ_3} ,$$

where C_{B3} is the capacitance at the base of Q_3 , and i_{BQ_3} is the maximum base current drive required for Q_3 .

The value of C_{B3} from the section on Gain and Bandwidth calculations is 78 pf. The maximum value of i_{BQ_3} would be 25.17 ma/ h_{FE3} . The current needed for the required slew rate at the base of Q_3 is then

$$I_{\text{req'd}} \geq 78 \text{ pf} (17.5 \text{ V}/\mu\text{sec}) + 25.17 \text{ ma}/550 ,$$

or

$$I_{\text{req'd}} \geq 1.4 \text{ ma} .$$

The input stage, Q_1 , in Figure 2, page 7, was therefore biased for a current of 2 ma in order to provide the current for the required slew rate at the base of Q_3 .

Gain and Bandwidth Calculations

As the slew rate is associated with the large-signal characteristics of the amplifier, there is no direct relationship between slew rate and small-signal bandwidth (3). The circuit must be designed with a wide bandwidth, however, to insure that bandwidth is not a slew rate limiting factor. The design goal of 10 nsec small- and large-signal rise time thus required a bandwidth of approximately 35 MHz.

The hybrid- π equivalent circuit, Figure 3, was used for the small-signal frequency analysis of the amplifier. Excellent discussions of this transistor model and its application in frequency analysis are given in References 10 and 15. The parameter nomenclature in Figure 3 is from Reference 10.

The open-loop gain of the amplifier of Figure 2, page 7, is the product of the gain of transistors Q_1 , Q_3 , and Q_5 , where the gain of Q_4 is assumed to be equal to the gain of Q_5 . The midband gain of a transistor stage is given by (10, 15)

$$A_{vt} \approx \frac{h_{FE} R_L}{R_i}, \quad (8)$$

where R_L is the equivalent load resistance at the collector of the transistor and R_i is the input resistance to the transistor.

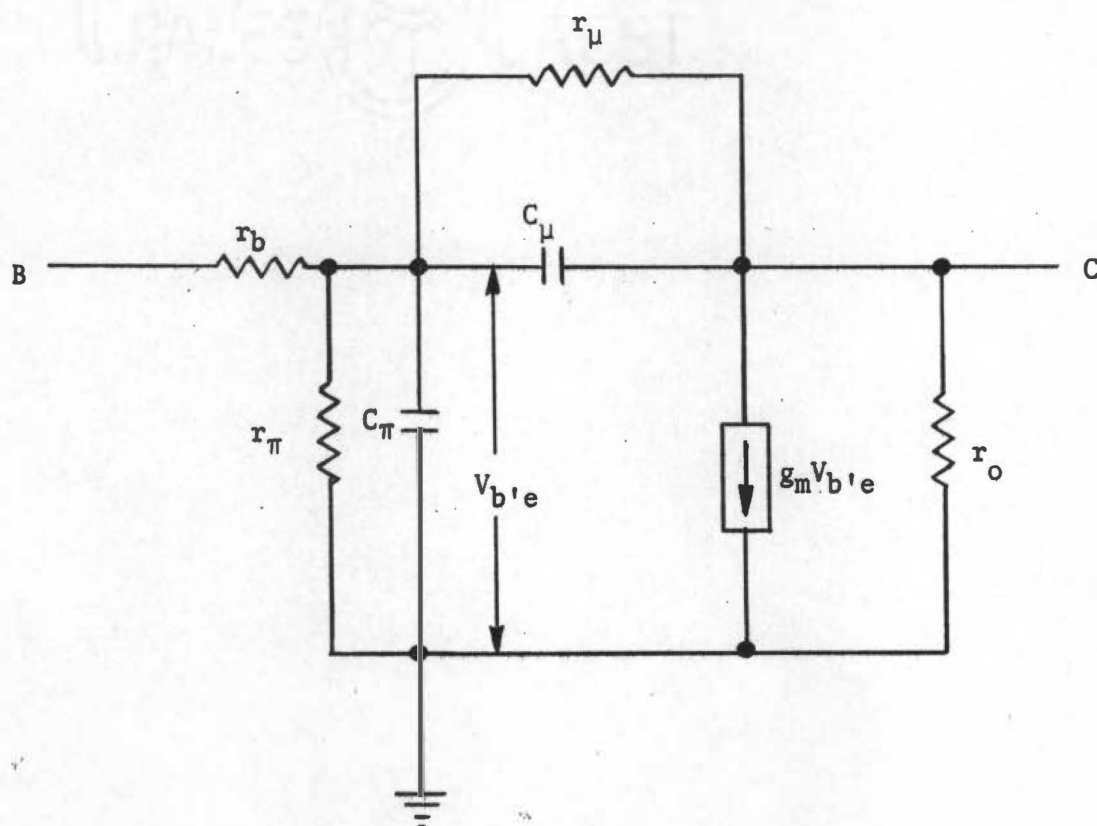


Figure 3. Transistor hybrid- π model (common emitter).

For Q_1 , Figure 2, page 7, we have

$$R_{L1} = R_2 // R_{i3} \quad (9)$$

where R_{i3} is the input resistance to Q_3 . Transistor input resistance is given by (10, 15)

$$R_i \approx r_\pi + (R_E) h_{FE} , \quad (10)$$

where r_π is given by (12, 14)

$$r_\pi = r_e h_{FE} ,$$

and R_E is any resistance from the transistor emitter to ground. Here, r_e is the emitter resistance of the transistor and, at a temperature of 25°C , is given as (10, 15)

$$r_e \approx \frac{26}{I_C \text{ (ma)}} \text{ ohms} , \quad (11)$$

where I_C is the quiescent collector current. Then for Q_3 in Figure 2, page 7, by substitution into Equation 11 the value of r_e is

$$r_{e3} = \frac{26}{12} = 2.16 \text{ ohms} .$$

With R_E equal to 25 ohms (R_6 in Figure 2, page 7), substitution into Equation 10, using a measured h_{FE} of 550, gives

$$R_{i3} = (2.16) 550 + 25 (550) .$$

$$R_{i3} = 15K .$$

By substitution in Equation 9

$$R_{L1} = \frac{(.5K)(15K)}{15.5K} = 490 \text{ ohms} .$$

Using Equations 10 and 11 with r_{e2} as R_E (10, 15), the input resistance of Q_1 is

$$R_{i1} = 2.6K .$$

Substitution into Equation 8 using a measured h_{FE} of 100 for Q_1 , Figure 2, page 7, gives the voltage gain of Q_1 as

$$A_{vt1} = 19 .$$

Using the same analysis for transistor Q_3 in the circuit of Figure 2, page 7, gives

$$A_{vt3} = 34.3 .$$

The gain of Q_4 , Figure 2, page 7, because of the common collector configuration, is approximately equal to 0.9 (10, 15). Therefore the total open-loop circuit gain is

$$A_{vt_{O.L.}} = (19)(34.3)(.9) .$$

$$A_{vt_{O.L.}} = 586 .$$

Expressed in decibels (d.b.) the gain of the circuit in Figure 2, page 7, is (10)

$$Avt_{d.b.} = 20 \log_{10} (Avt_{O.L.})$$

$$Avt_{d.b.} = 20 \log_{10} (5.86 \times 10^2)$$

$$Avt_{d.b.} = 20 (2.76) = 55.5 \text{ db}$$

The high open-loop gain of the amplifier in Figure 2 permits the closed-loop gain to be approximated by (2, 10)

$$Avt_{CL} = \frac{R_f}{R_5} + 1 \quad (12)$$

Substitution of the proper values into Equation 12 gives

$$Avt_{CL} = \frac{500}{50} + 1 = 11$$

or, as expressed in db,

$$Avt_{CL} = 20.8 \text{ db}$$

as the closed-loop amplifier gain.

The open-loop high-frequency -3db point of the amplifier, Figure 2, will be determined by the pole at the input to transistor Q_3 . This is due to the large input capacitance of this transistor (10, 15). The pole at the base of Q_3 has a break frequency of (10, 15)

$$f_{i3} \approx \frac{1}{2\pi R_t C_{B3}} \quad (13)$$

where C_{B3} is the total capacitance at the base of Q_3 and R_t is the equivalent resistance in parallel with C_{B3} .

The capacitance C_{B3} is the sum of $C_{\pi3}$, the reflected feedback capacitance C_R , the stray capacitance at the base of Q_3 , Figure 2, page 7, and the $C_{\mu1}$ of Q_1 . The reflected capacitance is given by (10, 15)

$$C_R = C_{\mu3} (1 + A_{vt3}) \approx C_{\mu3} (A_{vt3}) \quad (14)$$

Using the calculated A_{vt3} , and estimating $C_{\mu3}$ from the data sheet for the 2N5089 as the sum of $C_{cb} + C_{header} + C_{socket} \approx 1.3 \text{ pf} + 0.3 \text{ pf} + 0.2 \text{ pf} = 1.8 \text{ pf}$, and substituting in Equation 14

$$C_R \approx 1.8 \text{ pf} (34.3) = 61.7 \text{ pf} \quad .$$

$C_{\pi3}$ is obtained by (10, 15)

$$C_{\pi3} = \frac{1}{2\pi f_{\beta3} R_{i3}} \quad , \quad (15)$$

where $f_{\beta3}$ is the beta cutoff frequency for Q_3 . The beta cutoff frequency is obtained by (10, 15)

$$f_{\beta3} = \frac{f_{T3}}{\beta_3} \quad , \quad (16)$$

where f_{T3} is the current gain-bandwidth product for Q_3 , and β_3 is equal

to h_{FE3} . For the 2N5089, f_T was measured as 550 MHz at 12 ma and 15 volts. Substitution into Equation 16 yields

$$f_{\beta 3} = \frac{550 \times 10^6}{550} = 1.0 \text{ MHz} .$$

From Equation 15 then

$$C_{\pi 3} = \frac{.159}{(1 \times 10^6)(15 \times 10^3)} .$$

$$C_{\pi 3} = 10.6 \text{ pf} .$$

The total capacitance at the base of Q_3 then is approximately 78 pf with the assumption of 3 pf of stray capacitance and 2.8 pf as $C_{\mu 1}$.

Using Equation 13 with R_t equal to R_{L1} , the high frequency -3db point of the amplifier in Figure 2, page 7, is shown to be

$$f_{-3db} = \frac{1}{(2\pi)(72 \times 10^{-12})(.49K)} .$$

$$f_{-3db} = 4.5 \text{ MHz} .$$

Another pole, with a higher break frequency than the one at the base of Q_3 will be introduced by the capacitance at the collector of Q_3 , Figure 2. However, this is a second-order effect, as shown by Pierce and Paulus (17). Reference 17 indicates that a more exact calculation of the dominant poles of the circuit of Figure 2 produces two significant time constants, and if $\tau_1 \gg \tau_2$, then two dominant poles occur at

$$\tau_1 \approx R_t C_{B3} + R_{L3} C_{L3} , \quad (17)$$

and

$$\tau_2 \approx \frac{R_t R_{L3} [C_{\pi3} C_{\mu3} + C_{\pi3} C_{L3} + C_{L3} C_{\mu3}]}{\tau_1} . \quad (18)$$

R_{L3} is the resistance at the collector of Q_3 and C_{L3} is the capacitance at the collector of Q_3 . Using the above equations and substituting appropriate values gives

$$f_{-3db} \approx \frac{1}{2\pi\tau_1} = 3.45 \text{ MHz} .$$

and

$$f_{03} \approx \frac{1}{2\pi\tau_2} = 107 \text{ MHz} .$$

A plot of the open-loop gain magnitude vs. frequency for the circuit in Figure 2, page 7, is shown in Figure 4. Each pole in the circuit will cause a magnitude decrease of 6db per octave at frequencies above the break frequency of the pole (10, 15). Figure 4 indicates that the calculated gain magnitude vs. frequency plot would intersect the 20.8 db magnitude at a frequency slightly in excess of 100 MHz.

From Reference 2 we have that for the closed-loop amplifier, Figure 2, to be unconditionally stable, the closed-loop gain magnitude response (a straight line drawn at 20.8 db in Figure 4) must intersect the open-loop gain magnitude vs. frequency response at less than 12 db per octave. Figure 4 indicates an intersection of the closed-loop and open-loop curves near the location of the second pole where the open-loop

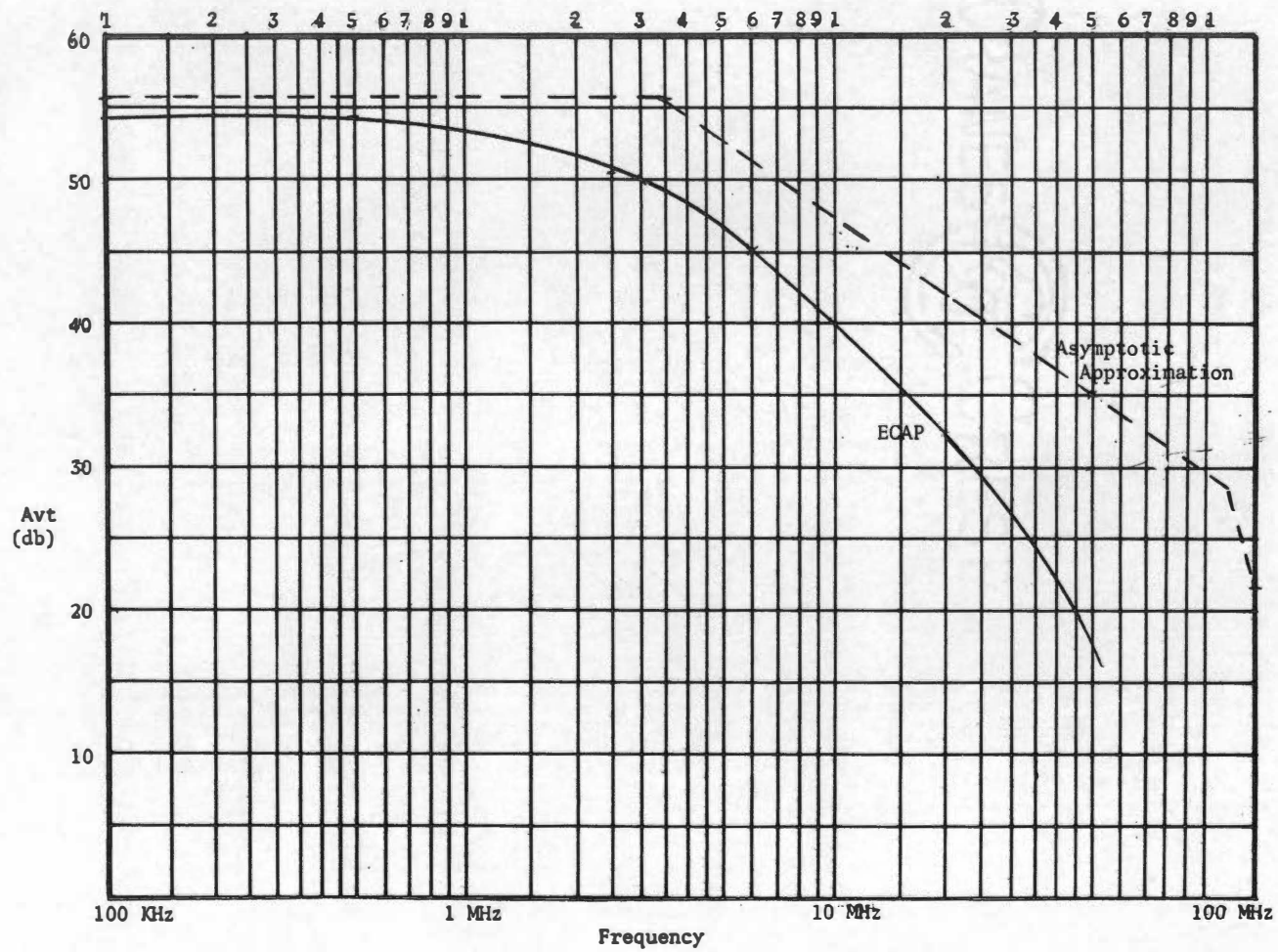


Figure 4. Open-loop magnitude vs. frequency plot for circuit in Figure 2, page 7.

response is approaching 12 db per octave. Because of this possibility that the circuit in Figure 2, page 7, could become unstable, a computer program, IBM's ECAP program (18), was used to obtain a gain magnitude vs. frequency response from the actual circuit equations and parameters.

ECAP requires a topological description of the circuit as its input with a transistor replaced by a current source and a resistive branch. The current through the resistive branch controls the direction and magnitude of the current source. The hybrid equivalent circuit was used for the analysis with the measured current gain values and specification sheet values for the other parameters used in the topological description of the circuit.

The result of the open-loop ECAP analysis is also shown in Figure 4. The slope of approximately 12 db per octave intersects the closed-loop gain, 20.8 db, at approximately 37 MHz. The phase shift of the open-loop output with respect to the input is shown by ECAP to be 180° at a frequency of approximately 40 MHz which is the frequency at which the circuit could possibly oscillate (2).

ECAP analyses were also obtained for the closed loop configuration of the circuit in Figure 2 with and without the bypass capacitor C_F . The closed loop results, shown in Figure 5, indicate that oscillation could be prevented by the addition of the capacitor C_F .

Although the desired small-signal bandwidth of 35 MHz could be realized in the circuit shown in Figure 2 the desired slew rate of 500 V/ μ sec, as shown in the accompanying section on Slew Rate Calculations, could not be attained. Also, the high current requirement of transistor

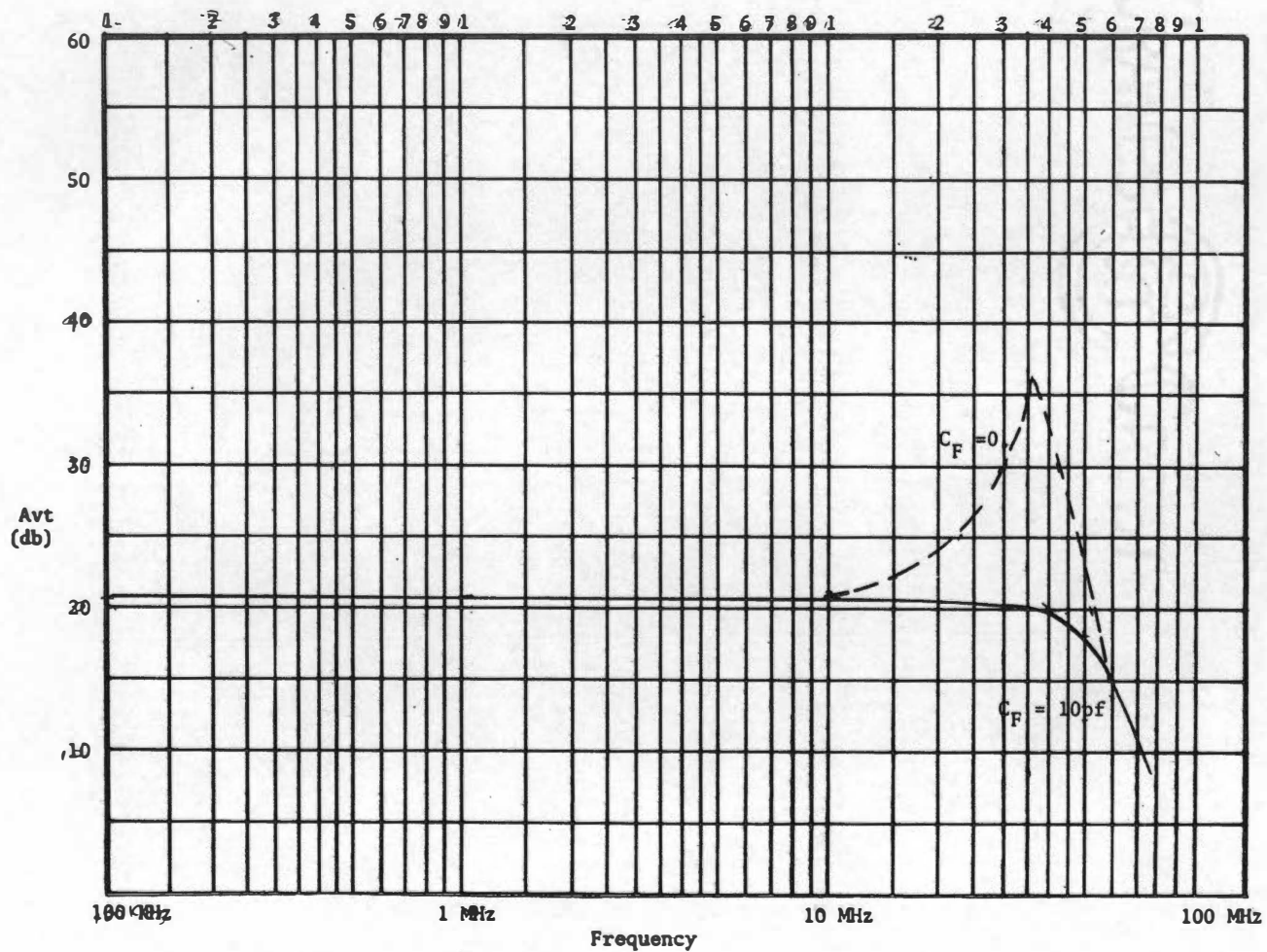


Figure 5. Closed-loop ECAP analysis of circuit in Figure 2, page 7.

Q_3 is an undesirable feature if the amplifier is to be used in a hybrid configuration with a linear IC amplifier. Since one of the goals of an IC design is low quiescent power dissipation, a method is needed to reduce the quiescent current flowing in Q_3 of Figure 2, page 7, without decreasing the circuit's slew rate.

CHAPTER III

COMPLEMENTARY AMPLIFIER WITH TRANSISTOR LOAD FOR PREDRIVER STAGE

The circuit shown in Figure 6 was designed to reduce the quiescent collector current of transistor Q_3 . R_7 in Figure 2, page 7, has been replaced by transistor Q_6 and its bias network. Also, by eliminating the large collector current swings previously required for Q_3 , a higher frequency transistor can now be utilized. The RF device, 2N3933, has a much higher f_T than the 2N5089, and, most importantly, a lower C_μ . A lower $C_{\mu 3}$ in Figure 6 is more desirable because of the added capacitance at the collector of Q_3 ($C_{\mu 6}$ of Q_6) and also because the dominant pole at the base of Q_3 is controlled by the Miller effect of Q_3 . Q_6 should be biased for a collector current of approximately 4ma in order to operate Q_3 near the optimum point on the f_T vs. I_C curve. This lower quiescent collector current for Q_3 is possible because the current contributed by the first two terms in Equation 4 is now supplied by the current source, Q_6 .

Capacitor C_1 was included in the circuit shown in Figure 6 to help speed up the transfer of charge through the C_T capacitance at the collector of Q_3 .

Transistor Q_6 will inject current into or remove current from the node at the collector of Q_3 , depending on the input signal polarity, on the fast transition portion of the input signal. The value for C_1 ,

10 pf, was determined experimentally to maximize the slew rate of the amplifier.

Slew Rate Calculations

Changing the value of $C_{\mu 3}$ to 0.55 pf, obtained from the 2N3933 specification sheet, and the addition of $C_{\mu 6}$, 2.6 pf as obtained from the 2N3906 specification sheet, in Equation 2 will give a value of 12.2 pf for C_T , the total capacitance at the collector of Q_3 in Figure 6. Substitution in Equation 3 yields a value of 7.3 ma as the required current to charge C_T for the desired slew rate of 500 V/ μ sec at the output. From Equation 4 the maximum collector current through Q_3 would then be the sum of 7.3 ma, plus the base current i_{BQ_5} of 1.2 ma, plus any standing current in Q_6 . However, since the signal from the base of Q_3 would turn-off Q_6 (for a negative output into R_L), this latter term is reduced. Hence, the maximum value of I_{C3} would be between 8.5 and 12.5 ma, or approximately 10 ma. A typical 2N3933 still has $f_T > 800$ MHz at this value of I_C .

For a positive output signal into R_L , Q_3 would tend to turn off, and indeed the minimum value of I_{C3} would be

$$I_{C(Q_3)Min} \approx I_{C3}(quiescent) - [i_{BQ_4} + i] ,$$

or

$$I_{C(Q_3)Min} \approx 4 \text{ Ma} - [8.5] \text{ ---> cutoff} ,$$

without the addition of C_1 . However, the leading edge of the signal at the base of Q_3 is coupled to the base of Q_6 to drive Q_6 and supply

the required current to charge C_T . In practice, since the f_T of Q_6 is significantly less than that of Q_3 , and only a small amount of charge is transferred through C_1 , one would still expect the slew rate to be greater for negative outputs than for positive outputs.

The slew rate requirement at the base of transistor Q_3 , Figure 6, page 27, will be reduced by a factor equivalent to the voltage gain of Q_3 as shown in Equation 6. From the section on Gain and Bandwidth calculations, page 30, the voltage gain of Q_3 in Figure 6 was estimated as 142. Substitution into Equation 6 yields 4.2 V/ μ sec as the required slew rate at the input to Q_3 .

The current required for the slew rate of 4.2 V/ μ sec at the input to Q_3 , Figure 6, can be calculated as before using Equation 3. Using the total capacitance at the base of Q_3 of 102 pf, obtained in the same manner as the total capacitance at the base of Q_3 in Figure 2, page 7, the maximum required current at the base of Q_3 , Figure 6, is

$$I_{\text{req'd}} \geq C_{B3} (4.2 \text{ V}/\mu\text{sec}) + i_{BQ_3} ,$$

or

$$I_{\text{req'd}} \geq 0.42 \text{ ma} + 10 \text{ ma}/550 \approx 0.44 \text{ ma} .$$

The input stage Q_1 of Figure 6 was therefore biased at a collector current of 0.5 ma.

Gain and Bandwidth Calculations

The calculations for the gain and bandwidth of the circuit shown in Figure 6, page 27, are basically the same as those for the circuit shown in Figure 2, page 7. The difference in calculations being that R_7 in Figure 2 is now replaced by $r_{oQ_6} [1 + g_{m_6} R_7]$ for calculations in the circuit shown in Figure 6 (10, 15). This value was obtained using the measured value of r_{oQ_6} for the 2N3906 used for Q_6 .

The calculated midband gain for the Q_3 and Q_1 stages was found to be approximately 142 and 9, respectively. Thus, the total open-loop gain was approximately $(9)(142)(0.9)$, or 1150 (61.2 db). The closed-loop gain, as before, is 20.8 db.

There are two significant high-frequency time constants, at the base of Q_3 and at the collector of Q_3 ; these were calculated to be 95 nsec and 55 nsec, respectively. Again using the second-order calculations of page 21 with $\tau_1 \gg \tau_2$ gives $\tau_1 \approx 150$ nsec and $\tau_2 \approx 7.4$ nsec. Hence the resulting poles occur at

$$f_{-3db} \approx \frac{1}{2\pi\tau_1} = 1.06 \text{ MHz}$$

and

$$f_{03} \approx \frac{1}{2\pi\tau_1} = 21.4 \text{ MHz}$$

The asymptotic approximation to the gain magnitude versus frequency response for the open-loop configuration of the circuit of Figure 6 is shown in Figure 7. Also included is the result of an ECAP

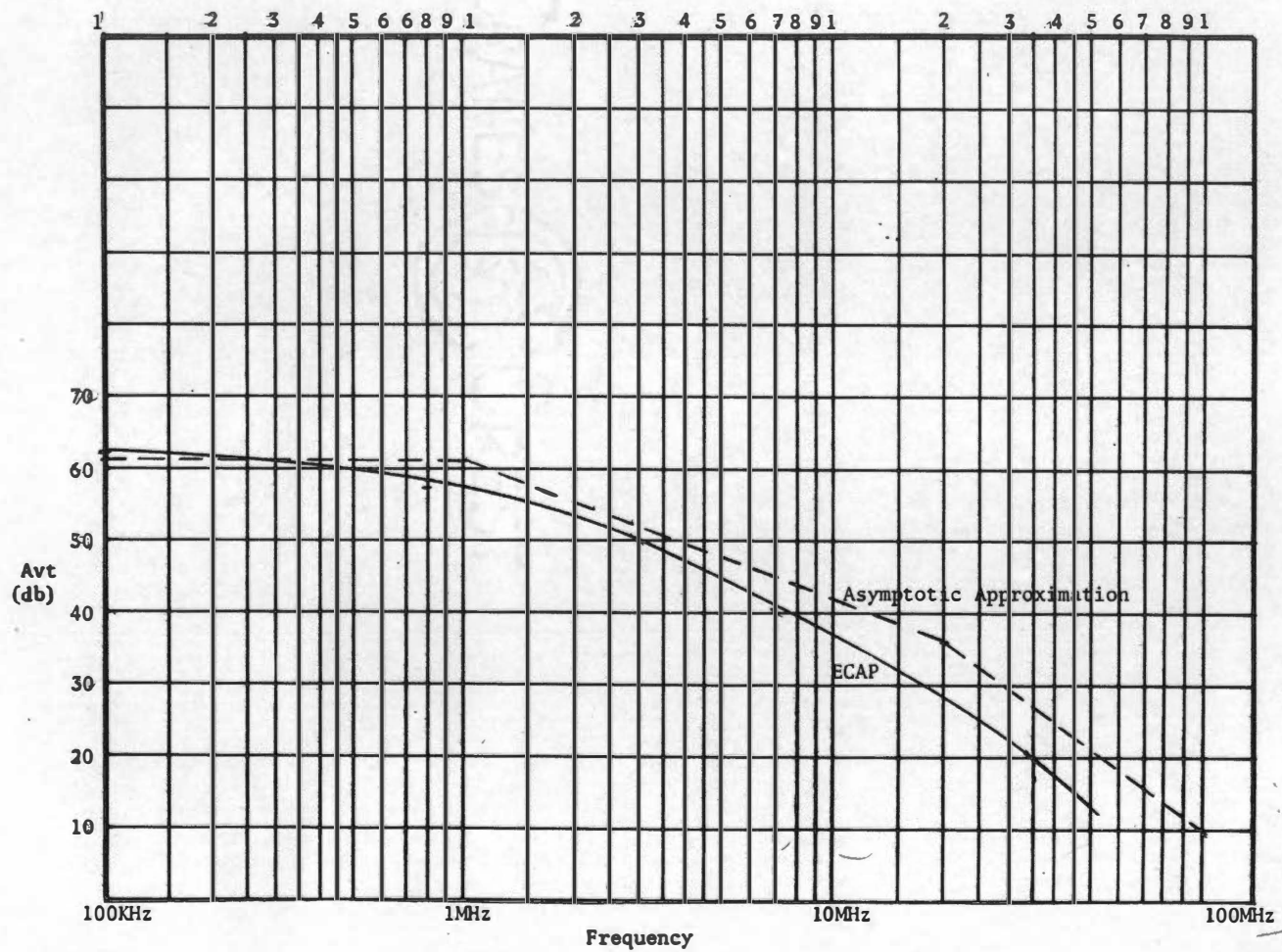


Figure 7. Open-loop magnitude vs. frequency plot for circuit in Figure 6, page 27.

analysis performed on the circuit, for comparison. The resulting closed-loop bandwidth for a closed-loop gain of 20.8 db is shown in Figure 7 to be approximately 35 MHz. The result of the ECAP analysis for the closed-loop amplifier of Figure 6, page 27, is shown in Figure 8.

The output transistors, Q_4 and Q_5 , in Figure 6 operate in the class-B mode. The transistors can be biased to operate class-A by the addition of two diodes in series between the collector of Q_6 and the collector of Q_3 .

Operating the output transistors class-A eliminates the crossover distortion caused when the output changes polarity. The quiescent current drain on the power supply is increased in the class-A configuration, however.

Noise Calculations

The hybrid- π equivalent circuit with associated noise sources, shown in Figure 9, was used for the noise analysis of the amplifier in Figure 6. An excellent discussion of this model and the noise sources is contained in References 10 and 19. The model in Figure 9 is for the midband frequency where the capacitance and r_{μ} effect of the hybrid- π circuit, Figure 3, page 15, are negligible (10, 19).

The total noise voltage on the output of a transistor stage can be reflected back to the transistor input as an equivalent noise voltage source divided by the gain of the transistor stage (10, 19). The noise voltage at the input to the amplifier in Figure 6 will be due mainly to the first stage, Q_1 and Q_2 .

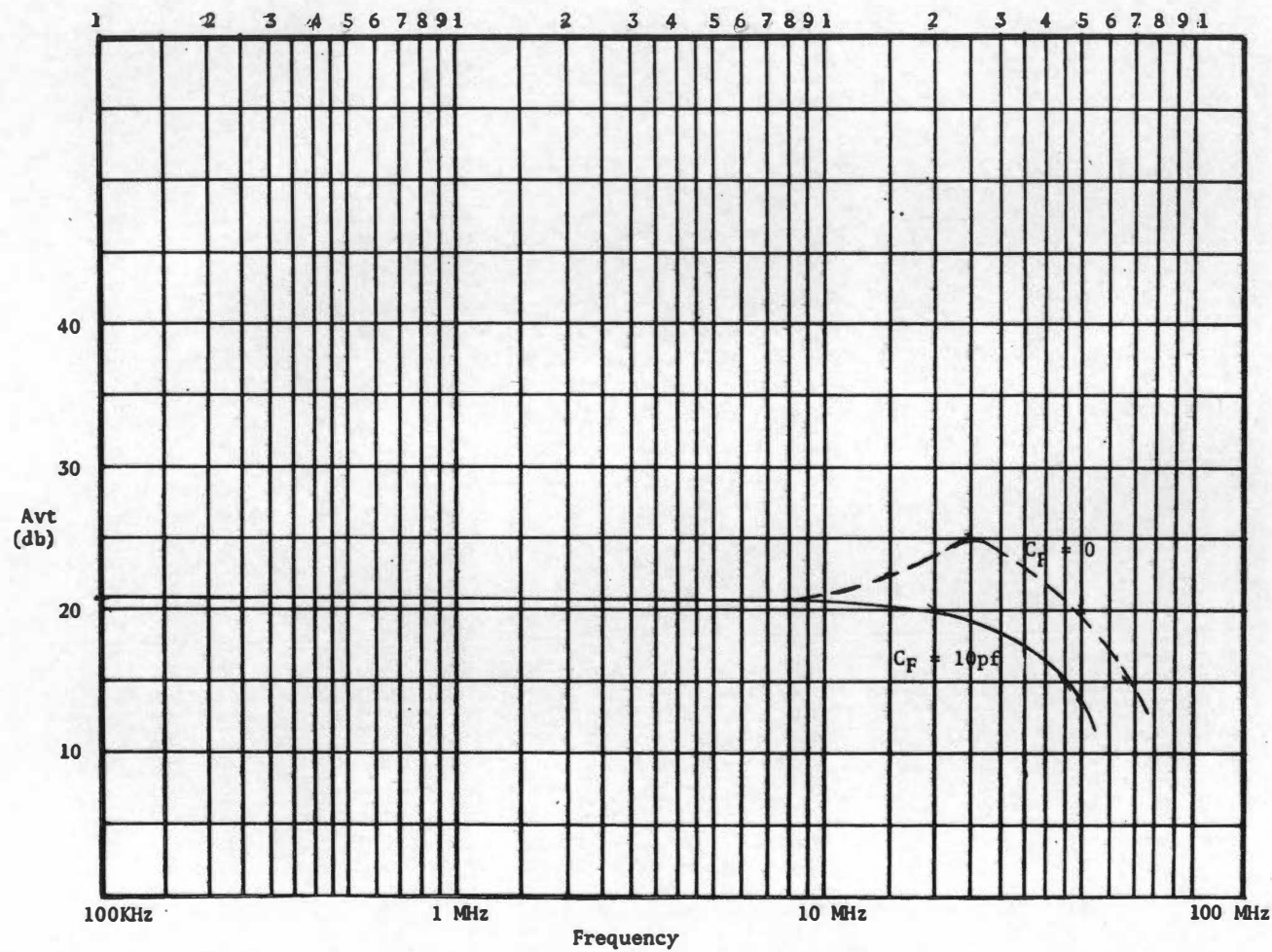


Figure 8. Closed-loop ECAP analysis of circuit in Figure 6, page 27.

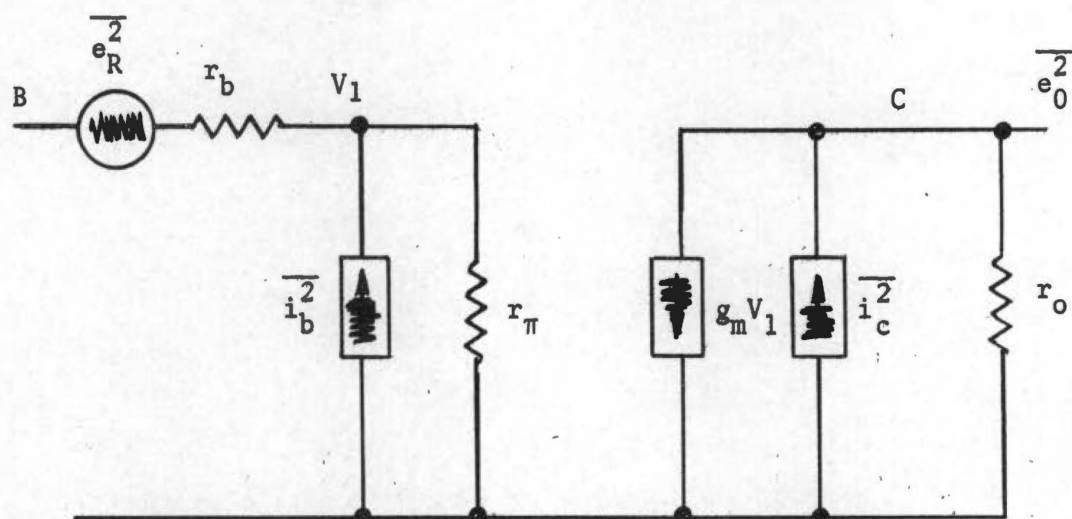


Figure 9. Noise model for a bipolar transistor (midband).

From References 10 and 19 we have the following for the input voltage noise source in Figure 9

$$\overline{e_R^2} = 4KT r_b \Delta f \text{ volts}^2, \quad (19)$$

where $\overline{e_R^2}$ is the mean square noise voltage of the source, K is the Boltzmann constant, T is the absolute temperature in degrees Kelvin, r_b is the value of the transistor base resistance, and Δf is the noise bandwidth. The current noise source at the input to the transistor stage is shown to be approximately (10, 19)

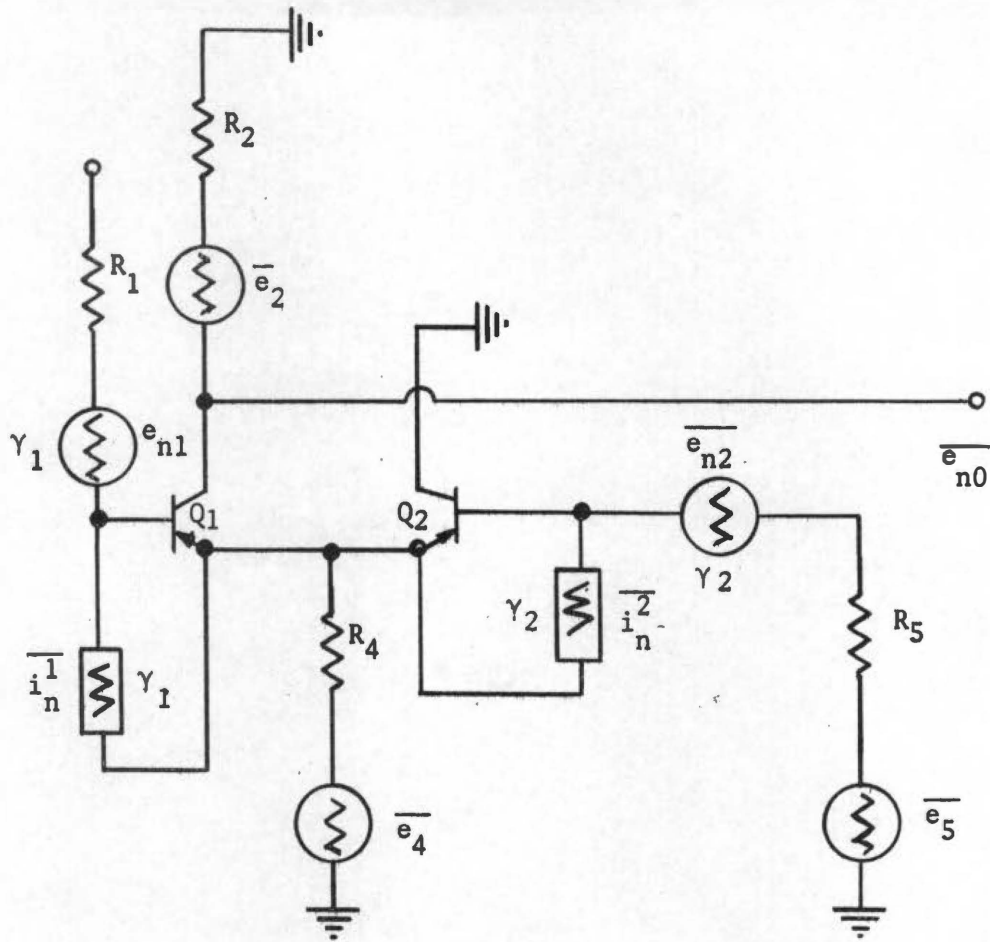
$$\overline{i_b^2} = 2qI_B \Delta f \text{ amps}^2, \quad (20)$$

while that at the output is

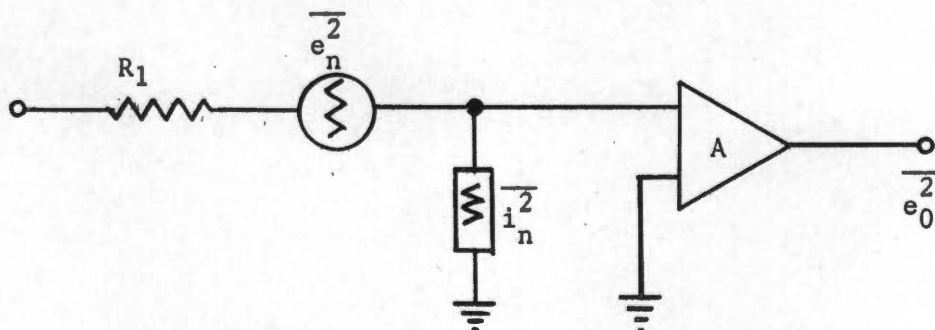
$$\overline{i_c^2} = 2qI_C \Delta f \text{ amps}^2, \quad (21)$$

where q is the value of electron charge, I_B is the base current, and I_C is the collector current.

The noise calculations are complicated by the fact that the input stage ($Q_1 - Q_2$) is a differential connection with both Q_1 and Q_2 contributing equal noise, since the gain from each to the output is identical. A complete diagram of the input differential stage with all the noise sources included as individual noise voltage or current generators is shown in Figure 10. A derivation of this circuit has been made in Reference (20) to obtain the total input noise as an equivalent input



(a) Complete circuit



(b) Equivalent representation of circuit (a)

Figure 10. Diagram of the differential amplifier input stage including noise sources.

voltage generator $\overline{e_n^2}$ in series with the input terminal and an equivalent input current generator $\overline{i_n^2}$ in parallel with the input, assuming zero correlation ($\gamma_1 = \gamma_2 = 0$) between the noise voltage and noise current generators and identical transistors ($\overline{e_{n1}} = \overline{e_{n2}}$, $\overline{i_{n1}} = \overline{i_{n2}}$, etc.).

The results of this derivation are

$$\begin{aligned} \overline{e_n^2} \approx 2 \left[\overline{e_{n1}^2} + r_e^2 \overline{i_{n1}^2} + \frac{\overline{e_5^2}}{2} + \frac{1}{2} \left(\frac{r_e}{R_4} \right)^2 \overline{e_4^2} \right. \\ \left. + 2 \left(\frac{r_e}{R_2} \right)^2 \overline{e_2^2} \right] \left(\frac{\text{Volts}^2}{\text{Hz}} \right) \end{aligned} \quad (22)$$

and

$$\begin{aligned} \overline{i_n^2} \approx \left[\overline{i_{n1}^2} + (\overline{e_{n1}^2} + \overline{e_5^2}) \left(\frac{1}{h_{FE1}} \right)^2 \left(\frac{1}{R_4} \right)^2 + \frac{\overline{e_4^2}}{R_4} \left(\frac{1}{h_{FE1}} \right)^2 \right. \\ \left. + \left(\frac{\overline{e_2^2}}{R_2^2} \right) \left(\frac{1}{h_{FE1}} \right)^2 \right] \left(\frac{\text{amp}^2}{\text{Hz}} \right), \end{aligned} \quad (23)$$

or, for all practical purposes,

$$\overline{i_n^2} \approx \overline{i_{n1}^2} \quad (24)$$

In the above equations it is shown (20) that good approximations to $\overline{e_{n1}^2}$, $\overline{i_{n1}^2}$, etc., are (in units of volts^2/Hz and amp^2/Hz),

$$\overline{e_{n1}^2} \approx 4K_t \left[r_{b1} + \frac{r_{e1}}{2} \right]$$

$$\overline{i_{n1}^2} \approx 2qI_{B1}$$

$$\overline{e_5^2} = 4KTR_5$$

$$\overline{e_4^2} = 4KTR_4$$

$$\overline{e_2^2} = 4KTR_2 \quad (25)$$

Thus, Equations 22 and 24 reduce to

$$\begin{aligned} \overline{e_n^2} \approx 4kT \left[2r_{b1} + R_5 + R_2 \left(\frac{2r_e}{R_2} \right)^2 + r_{e1} \right. \\ \left. \left(1 + \frac{r_{e1}}{R_4} + \frac{1}{2h_{FE1}} \right) \right] \overline{\text{Volt}^2/\text{Hz}} \end{aligned} \quad (26)$$

and

$$\overline{i_n^2} \approx 2qI_{B1} \overline{\text{amp}^2/\text{Hz}} \quad (27)$$

Substituting values from the circuit of Figure 6, page 27, and including the noise of R_1 , the total equivalent input noise for the amplifier is approximately

$$\overline{e_{in}^2} \approx 4kTR_1 + \overline{e_n^2} + \overline{i_n^2} R_1^2,$$

or (if $r_{b1} = r_{b2} \approx 100$ ohms, estimated)

$$\overline{e_{in}^2} \approx 4kT[370 \text{ ohms}] \approx 6 \times 10^{-18} \text{ (volt}^2\text{/Hz)} . \quad (28)$$

Hence, the equivalent input noise contributed by the transistors and resistors is

$$\overline{e_{in}} \approx 2.5 \text{ nV}/\sqrt{\text{Hz}} . \quad (29)$$

From reference (19) the equivalent noise bandwidth for a single-pole network is

$$\Delta f = \pi/2 f_{-3db} , \quad (30)$$

or for a bandwidth of 35 MHz for the amplifier of Figure 6, page 27, $\Delta f \approx 55$ MHz. Thus, the total equivalent input noise of the amplifier from Eq. (29) is

$$\overline{e_{in}} \approx 18.5 \text{ } \mu\text{V (rms)} . \quad (31)$$

This calculation assumes that, since the gain of $Q_1 - Q_2$ is reasonably large (~ 9) that noise contributed by $Q_3 - Q_6$ and R_f will be negligible.

CHAPTER IV

EXPERIMENTAL RESULTS

The output stage of the amplifier used to amplify pulses or wideband data must provide bipolar output signals with a high slew rate, a wide bandwidth, and good linearity. A check of these operating characteristics is therefore mandatory.

As the desirable results would produce output rise times near 10 nsec, a pulse generator which could provide both positive and negative inputs with rise times of approximately 1 nsec was used to provide the input signal. A sampling scope was used to provide an accurate measurement and presentation of the amplifier output signals. A radio-frequency generator provided the necessary input for the closed loop frequency response measurement.

Prior to all measurements, resistor R_4 in Figure 6, page 27, was adjusted to provide an output of zero volts with the input shorted to ground.

All experimental results were accumulated on the circuit in Figure 6. The circuit shown in Figure 2, page 7, was not constructed because of the conclusion arrived at in Chapter II that this circuit would not meet the slew rate requirements.

Figure 11 shows the measured closed-loop frequency response of the amplifier for both the class-A and class-B bias conditions. The bandwidth of the class-A bias condition is, from Figure 11, approximately

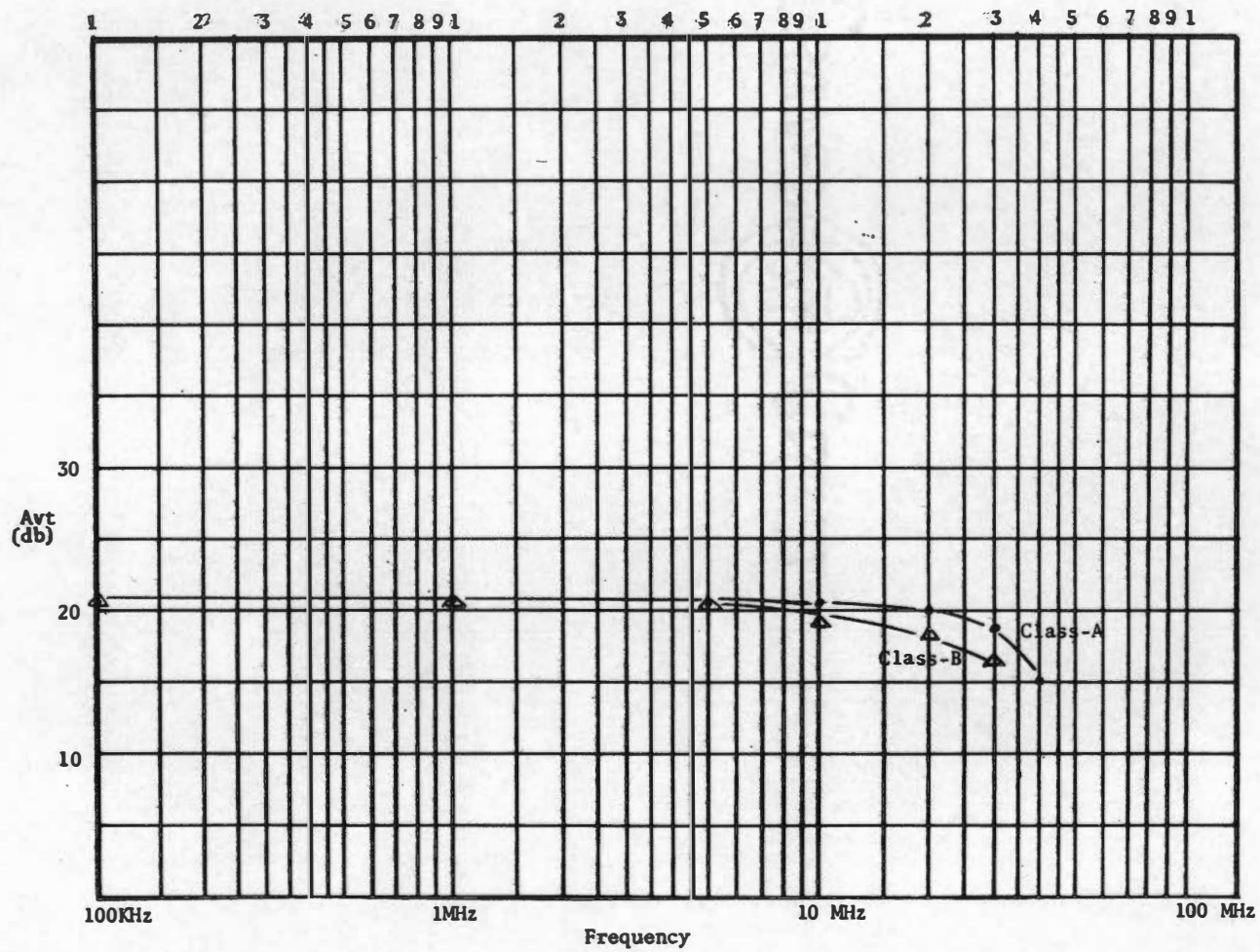


Figure 11. Measured small-signal frequency response for circuit in Figure 6, page 27.

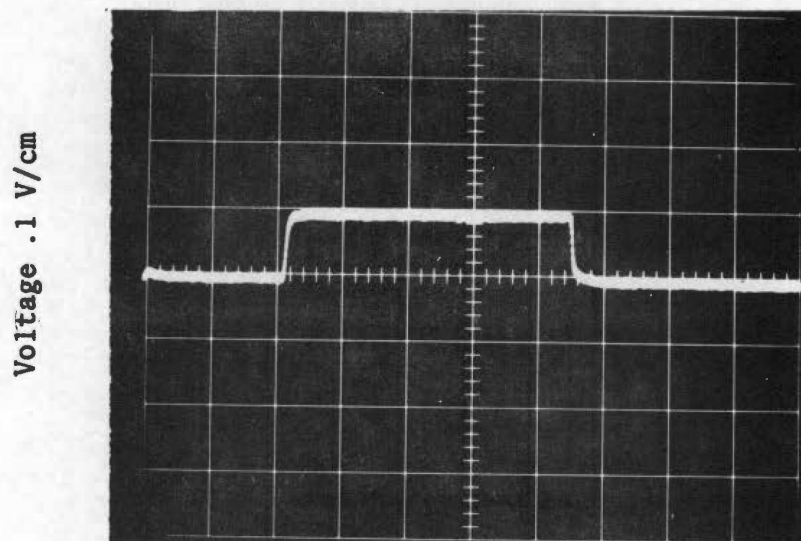
35 MHz while that for the class-B bias condition is approximately 28 MHz.

Figures 12 and 13 show the input and output for the class-B mode of operation for small-signal inputs. The crossover distortion characteristic of the class-B complementary amplifier (13) is evident in the positive output shown in Figure 12. The small-signal rise time, obtained from Figure 13 because of the crossover distortion in Figure 12, of approximately 12 nsec corresponds to a small-signal bandwidth of 29 MHz (11) for the class-B biased configuration, which agrees with the value of 28 MHz above.

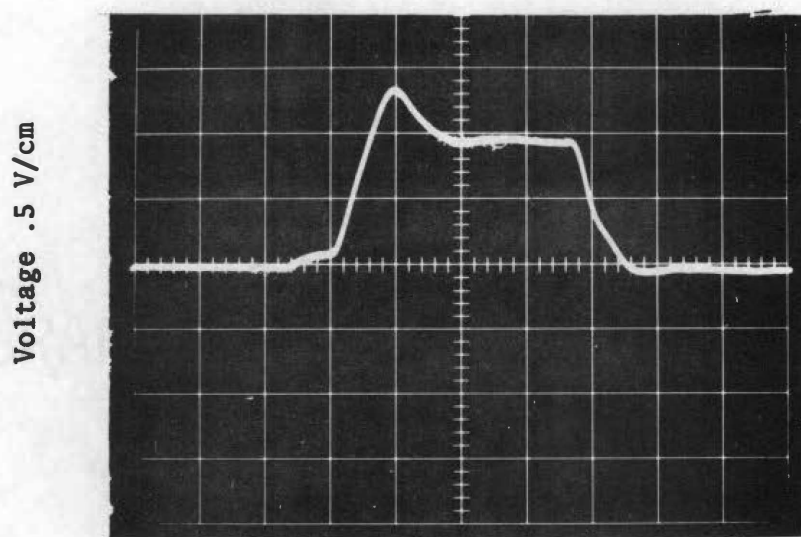
Figures 14 and 15 show the input and output for the class-A mode of operation for small-signal inputs. The small-signal rise time of approximately 10 nsec corresponds to a small-signal bandwidth of 35 MHz (11) for the class-A biased configuration.

The above observations indicate excellent agreement between the measured small-signal bandwidth and measured small-signal rise time for both bias conditions. The class-B bandwidth, however, is approximately 7 MHz lower than the predicted results of 35 MHz, Figure 8, page 33, whereas the class-A bandwidth compares well with the predicted results of 35 MHz, Figure 8.

Figures 16 and 17 show the amplifier input and output for the class-B mode of operation for large-signal output drive to ± 5 volt. As the slew rate of the amplifier was not anticipated to be the same for positive and negative outputs, the slew rate of the amplifier was measured for both conditions. The output slew rate for the class-B

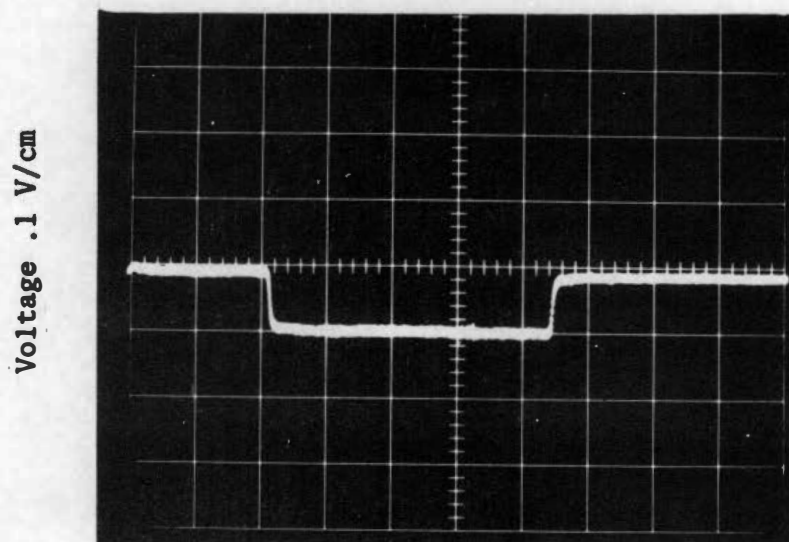


(a) Input Time 20 nsec/cm



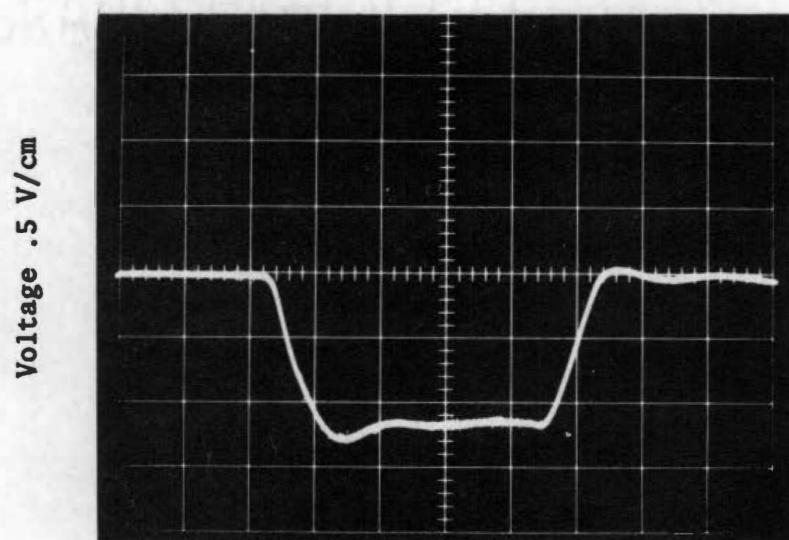
(b) Output Time 20 nsec/cm

Figure 12. Circuit waveforms for positive small-signal input class-B.



(a) Input

Time 20 nsec/cm



(b) Output

Time 20 nsec/cm

Figure 13. Circuit waveforms for negative small-signal input class-B.

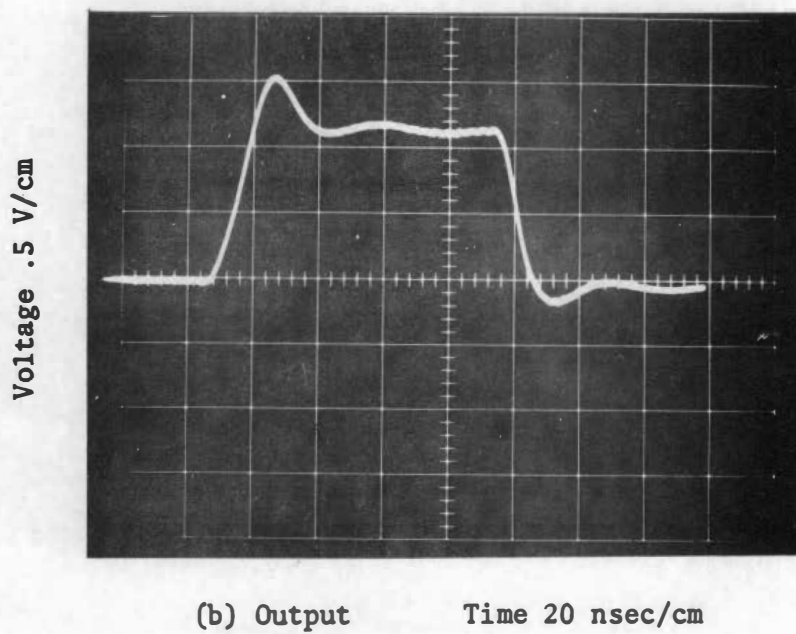
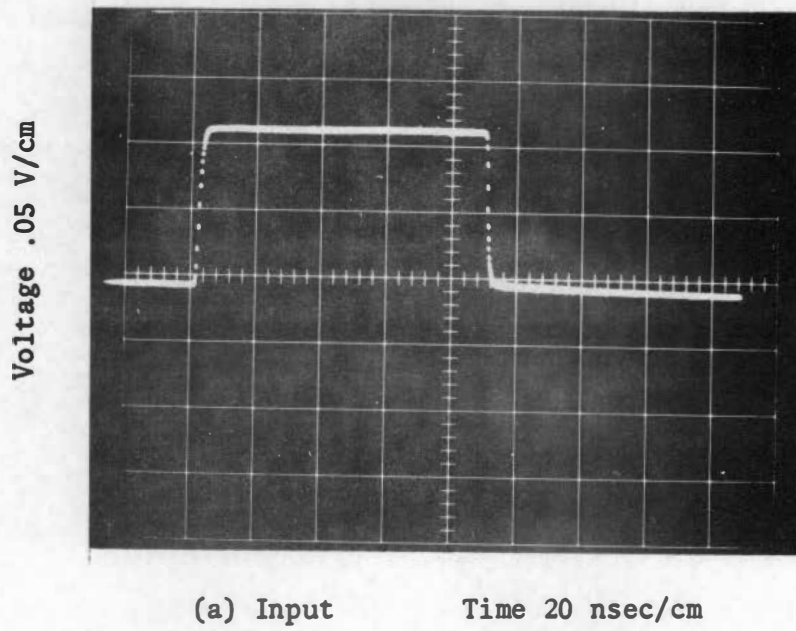
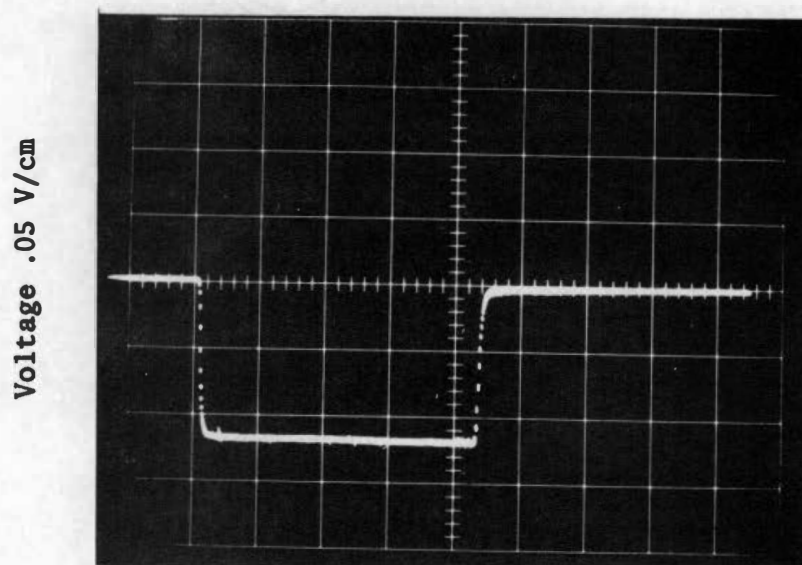
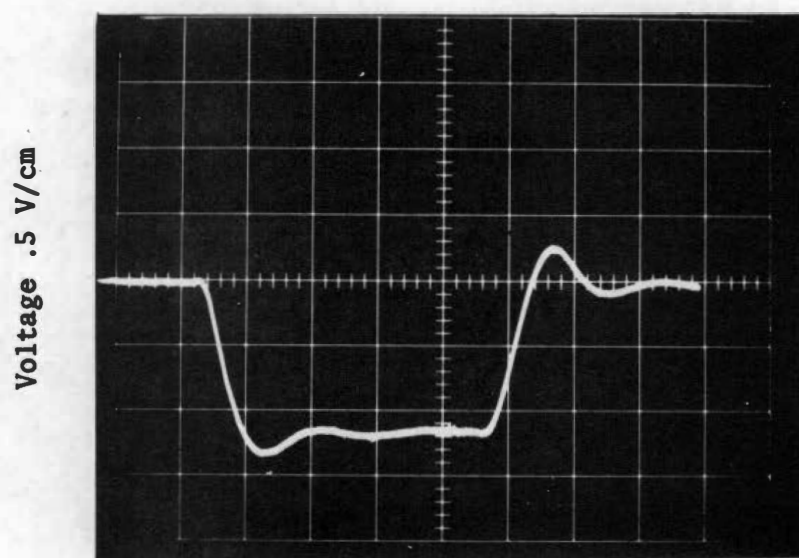


Figure 14. Circuit waveforms for positive small-signal input class-A.



(a) Input

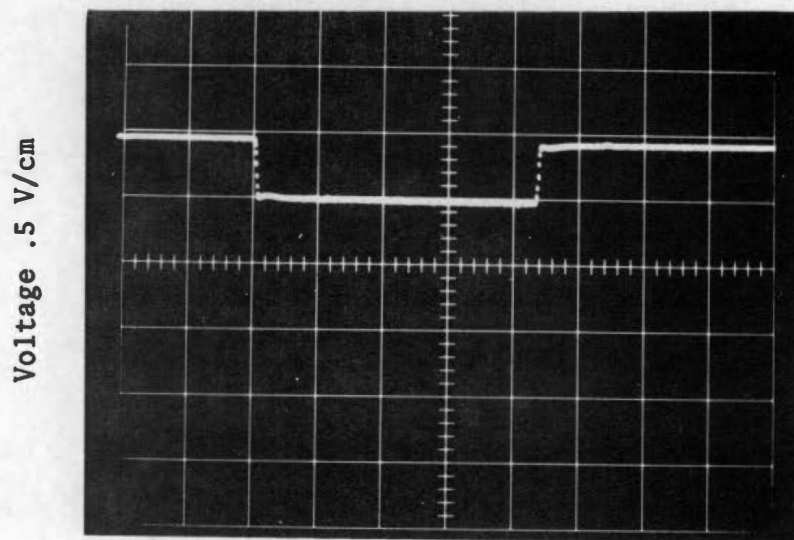
Time 20 nsec/cm



(b) Output

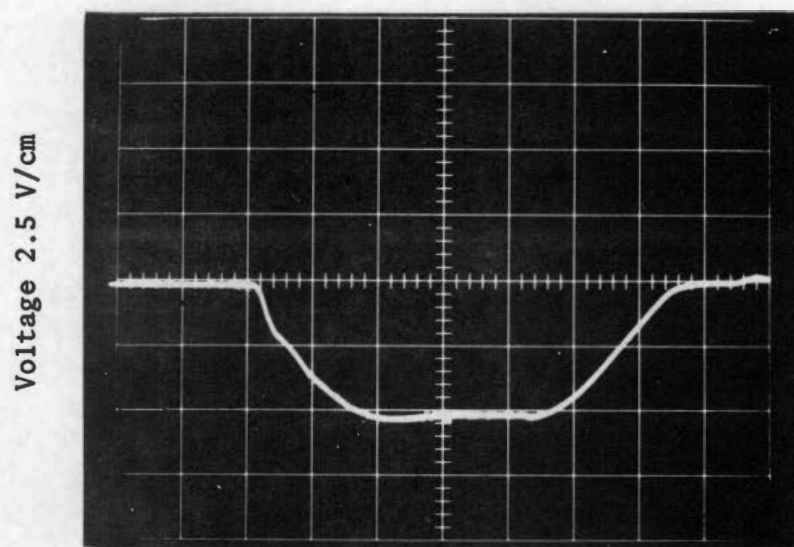
Time 20 nsec/cm

Figure 15. Circuit waveforms for negative small-signal input class-A.



(a) Input

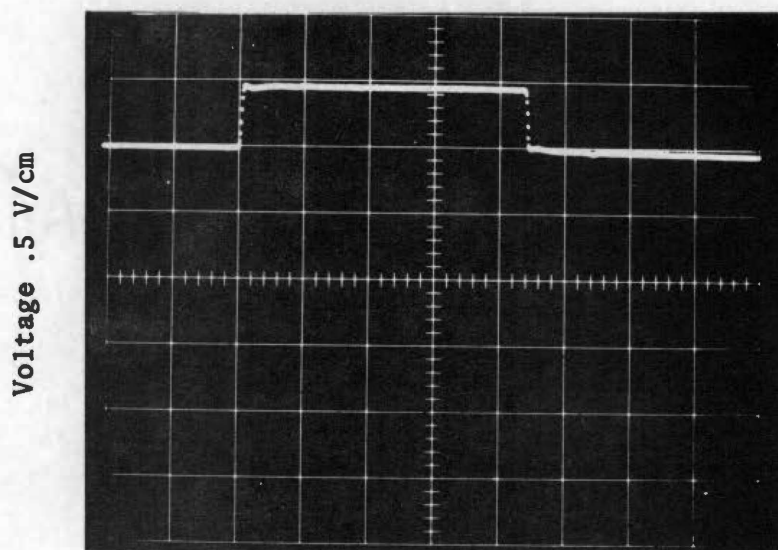
Time 20 nsec/cm



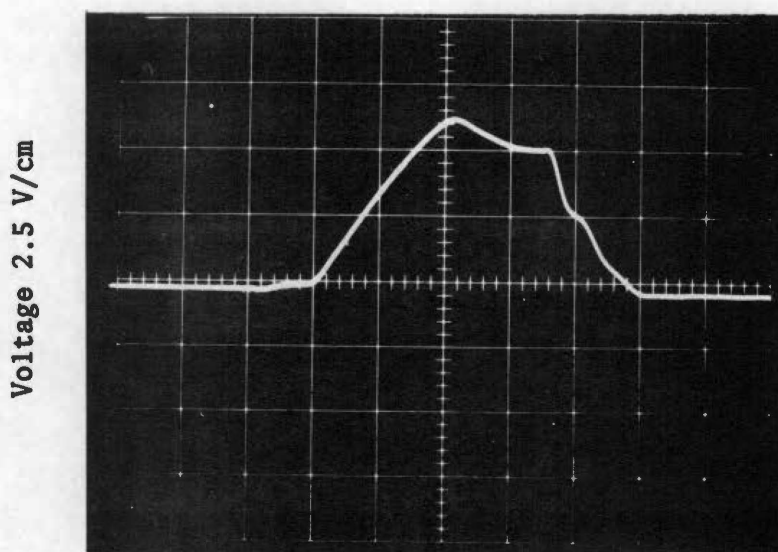
(b) Output

Time 20 nsec/cm

Figure 16. Circuit waveforms for negative large-signal input class-B.



(a) Input Time 20 nsec/cm



(a) Output Time 20 nsec/cm

Figure 17. Circuit waveforms for positive large-signal input class-B.

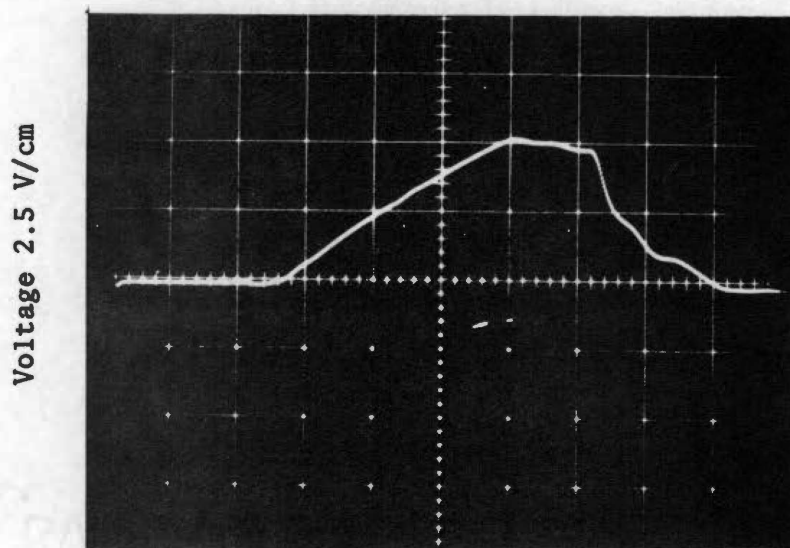
configuration was measured as approximately 175 V/ μ sec and 160 V/ μ sec for negative and positive inputs, respectively.

In order to demonstrate the effects of the coupling capacitor C_1 in Figure 6, page 27, the large-signal circuit output was observed in the class-B bias condition with the coupling capacitor removed from the circuit. The results, as shown in Figure 18, indicate a slew rate of 100 V/ μ sec and 91 V/ μ sec for negative and positive inputs respectively. Thus, a reduction of approximately 75 V/ μ sec occurred.

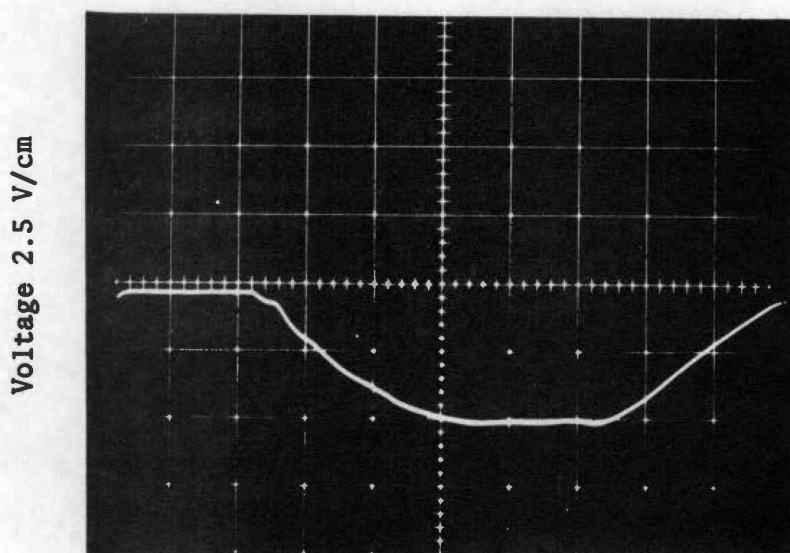
Figure 19 shows the maximum frequency at which the full output drive and large-signal gain could be maintained without excessive distortion of the output signal. The class-B output signal clearly shows the crossover distortion associated with this bias condition. The inputs for both Figure 19(a) and 19(b) were 0.5 V peak sine waves.

The slew rate was also measured with the output biased in the class-A mode. Figure 20 shows the output for a negative input signal and Figure 21 shows the output for a positive input signal. The slew rate, as determined from these figures, is approximately 200 V/ μ sec and 170 V/ μ sec for negative and positive inputs respectively.

A qualitative indication of the linearity of the amplifier was obtained by applying a series of positive and negative pulses with varying amplitudes and measuring the amplitude of the output signal. Figure 22 is a plot of the amplifier output amplitude vs. input amplitude for both class-A and class-B bias conditions.



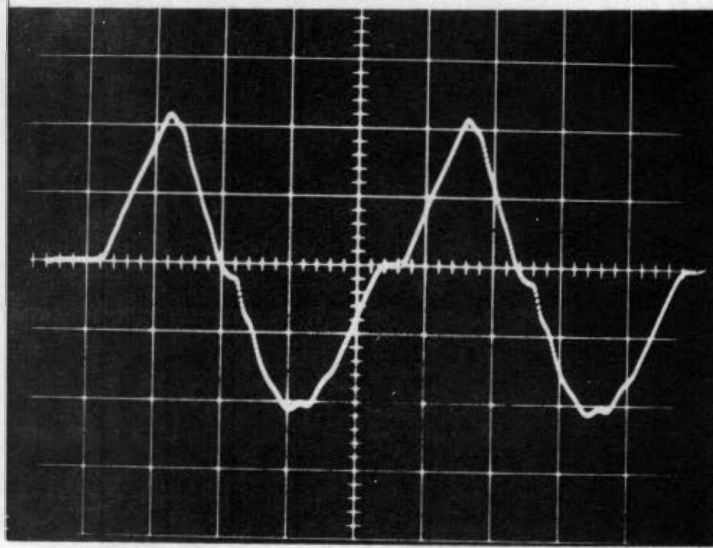
(a) Positive Output Time 20 nsec/cm



(b) Negative Output Time 20 nsec/cm

Figure 18. Circuit output with capacitor C_1 removed, class-B.

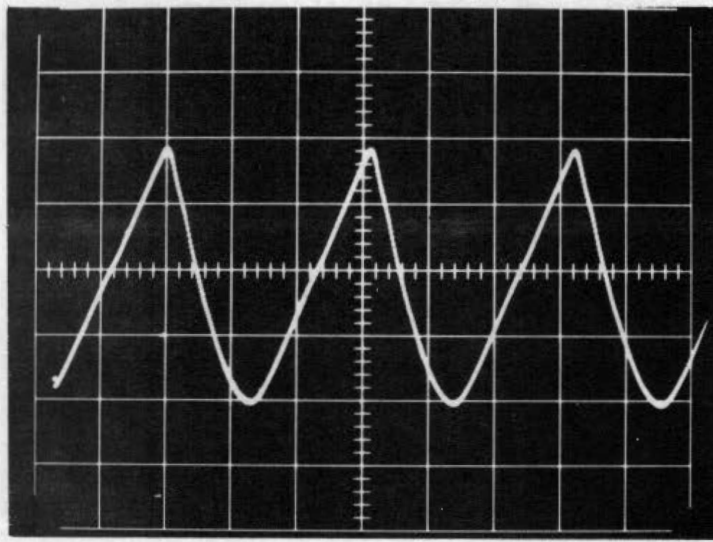
Voltage 2.5 V/cm



(a) Class-B

Time 25 nsec/cm

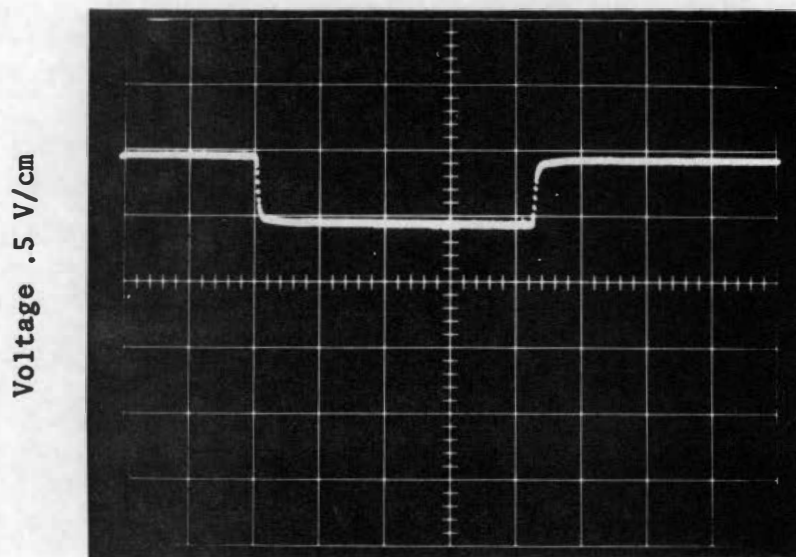
Voltage 2.5 V/cm



(b) Class-A

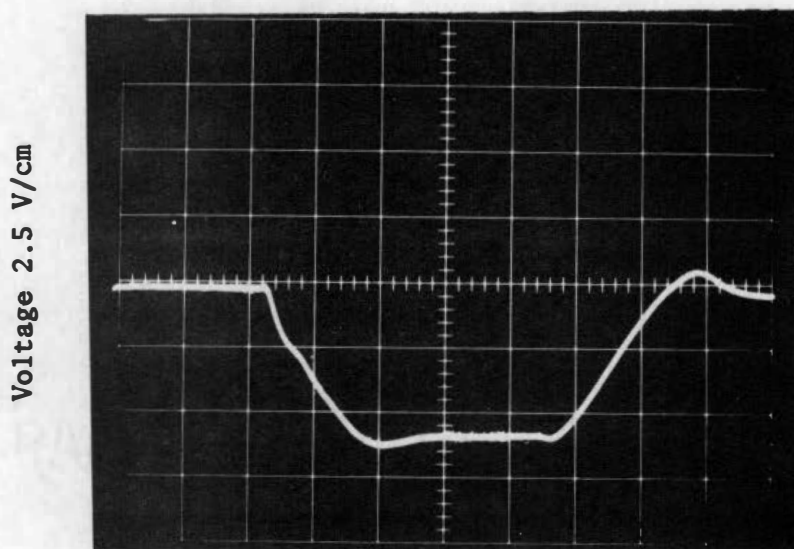
Time 25 nsec/cm

Figure 19. Full-power sine wave output.



(a) Input

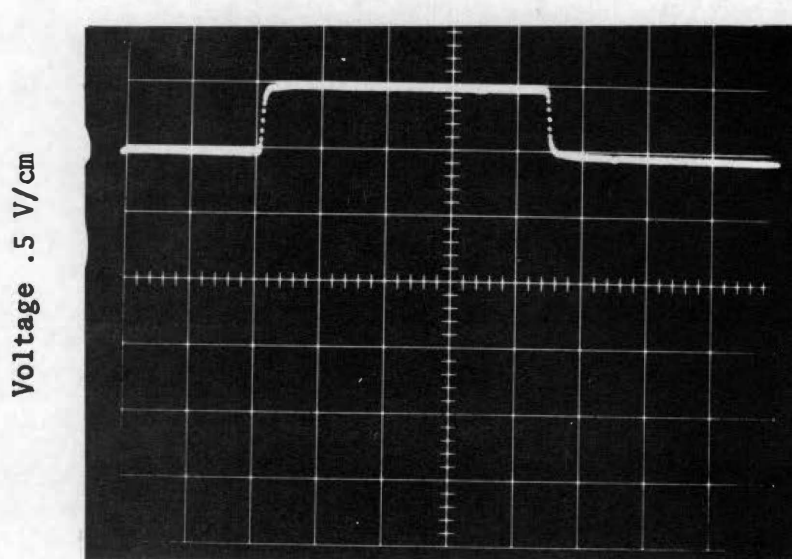
Time 20 nsec/cm



(b) Output

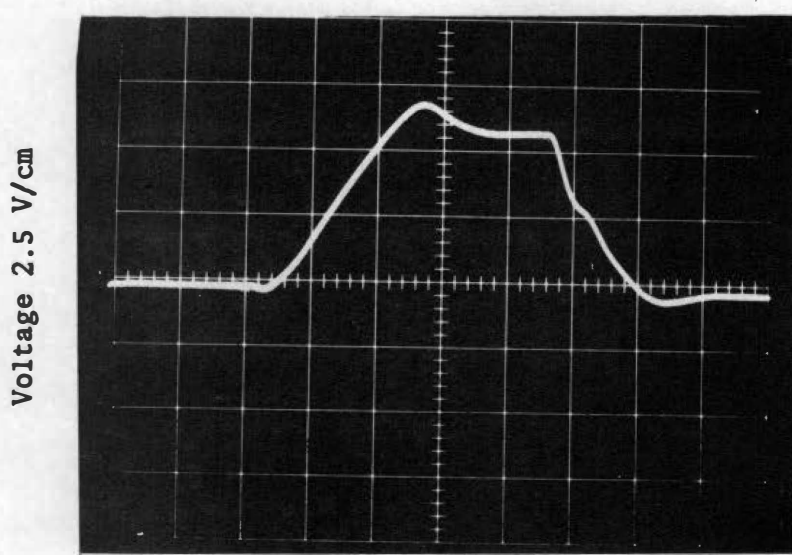
Time 20 nsec/cm

Figure 20. Circuit waveforms for negative large-signal input, class-A.



(a) Input

Time 20 nsec/cm



(b) Output

Time 20 nsec/cm

Figure 21. Circuit waveforms for positive large-signal input, class-A.

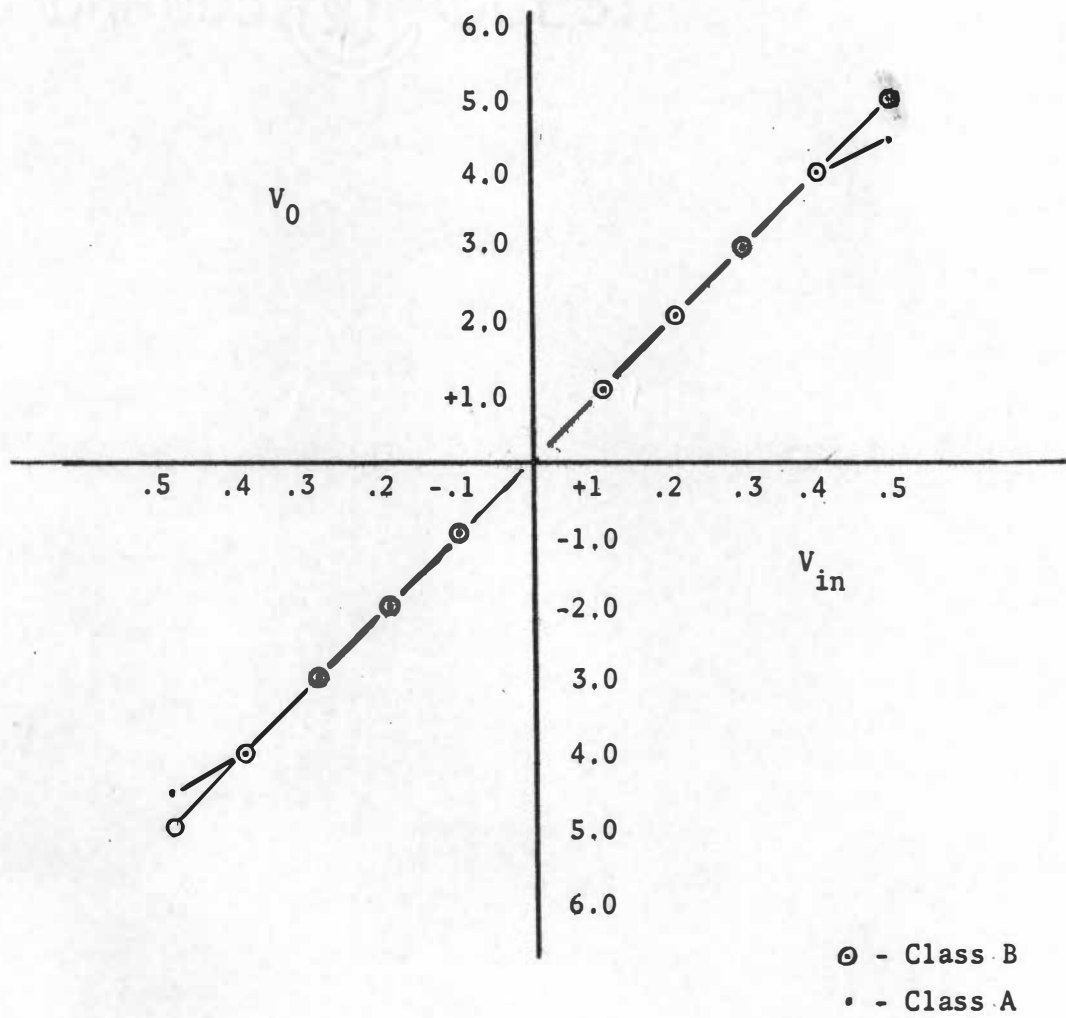


Figure 22. Amplifier linearity.

CHAPTER V

CONCLUSIONS

The improvement of the slew rate of an IC amplifier can be accomplished by a hybrid configuration of the IC and a single npn-pnp complementary stage. All components of the circuit with the exception of the two output transistors, the predriver stage and the capacitors could be included as part of the IC.

This thesis reports the design of a complementary output stage. All design objectives were achieved except the desired slew rate of 500 V/ μ sec for the large-signal output. This was due to the relatively simple linear approximations utilized to estimate required currents in the transistor stages. A more complete analysis of slew rate limitations would require a nonlinear model for the transistor.

If faster slew rates are required, additional stages and circuit complexity such as that described in reference 6 would be required. Another technique would be to reduce the capacitance at the output of the predriver by having the predriver drive a complementary pair of high-frequency transistors whose common-emitter output would drive the complementary output pair. Both of the above configurations, however, increase the circuit complexity and cost.

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LIST OF REFERENCES

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